1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
03		268628	ENGINEERING RELEASED	03/28/03	?

NIMITZ

03/14/2003

PAGE	CONTENTS
1	TITLE PAGE AND CONTENTS
2	SYSTEM BLOCK DIAGRAM
3	POWER BLOCK DIAGRAM
4	PCB NOTES AND HOLES
5	MPC7450 MAXBUS INTERFACE
6	MPC7450 DATA
7	CPU PLL AND CONFIGURATION STRAPS
8	INTREPID MAXBUS AND BOOT STRAPS
9	INTREPID MEMORY INTERFACE / BOOT ROM
10	DDR MEMORY MUXES
11	200PIN DDR MEMORY SODIMM CONNECTORS
12	INTREPID AGP 4X/PCI
13	INTREPID ENET/FW/UATA/EIDE INTERFACES
14	INTREPID GPIOS/SERIAL/USB INTERFACES/SSCG
15	INTREPID POWER RAILS
16	INTREPID DECOUPLING
17	CARDBUS CONTROLLER (PCI1510)
18	MAP31 AGP & FRAME BUFFER
19	MAP31 LVDS/TMDS/GPIO & GPU VCORE
20	MAP31 ANALOG, DVO INTERFACE, GND
21	VIDEO CONNECTORS - INVERTER, DVI, S-VIDEO DUAL-CHANNEL LVDS

PAGE	CONTENTS
22	LMU, LIGHT SENSOR, BOOTBANGER, SLEEP LED SPIDEY - KBD,TPAD,HALL EFFECT,PWR BUTTON
23	INTERNAL CONNECTORS - DVD, CARDSLOT, HARD DRIVE, LEFT USB/BLUETOOTH
24	FAN CONTROLLER, MODEM, SOUND SERIAL DEBUG (JOLLY ROGER, PWR/NMI/RESET)
25	USB 2.0
26	MARVELL GIGABIT ETHERNET PHY
27	FIREWIRE A/B PHY
28	FIREWIRE A/B CONNECTORS, PORT POWER LIMITER
29	PMU (POWER MANAGEMENT UNIT)
30	BATTERY CHARGER AND CONNECTOR
31	12.8V SYSTEM POWER SUPPLY / PMU POWER SUPPLY
32	3.3V / 5V SYSTEM POWER SUPPLIES
33	CPU CORE VOLTAGE POWER SUPPLY
34	1.5V/ 1.8V / 2.5V SYSTEM POWER SUPPLIES
35	SIGNAL CONSTRAINTS (1 OF 3) - DIGITAL/CLK
36	SIGNAL CONSTRAINTS (2 OF 3) - DIGITAL/DIFF
37	SIGNAL CONSTRAINTS (3 OF 3) - POWER NETS
38	FUNCTIONAL TEST POINTS
39	REVISION HISTORY (1 OF 1)
40-41	SIGNAL NAMES
42-43	COMPONENT LOCATIONS

BOM OPTIONS	STUFF	NO STUFF
D3_HOT		√
D3_COLD	√	
GPU_SS	√	
GPU_SWITCH	√	
SERIAL_DEBUG	√	
VCORE_OFFSET		√
1_8V_MAXBUS	√	
1_5V_MAXBUS		√
NEC_USB	√	
INTREPID_USB		√
BBANG		√
NO_BBANG	√	
MAP31	√	
MAP17		√
SSCG		√
NO_SSCG	√	
5V_HD_LOGIC	√	
3V_HD_LOGIC		√

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6443	1	SCHEM,MLB,PB 17	SCH1	
820-1511	1	PCBF,MLB,PB 17	PCB1	

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE NONE	

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

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TITLE
SCHEM,NIMITZ,Q41

DRAWING NUMBER 051-6443 REV. 03

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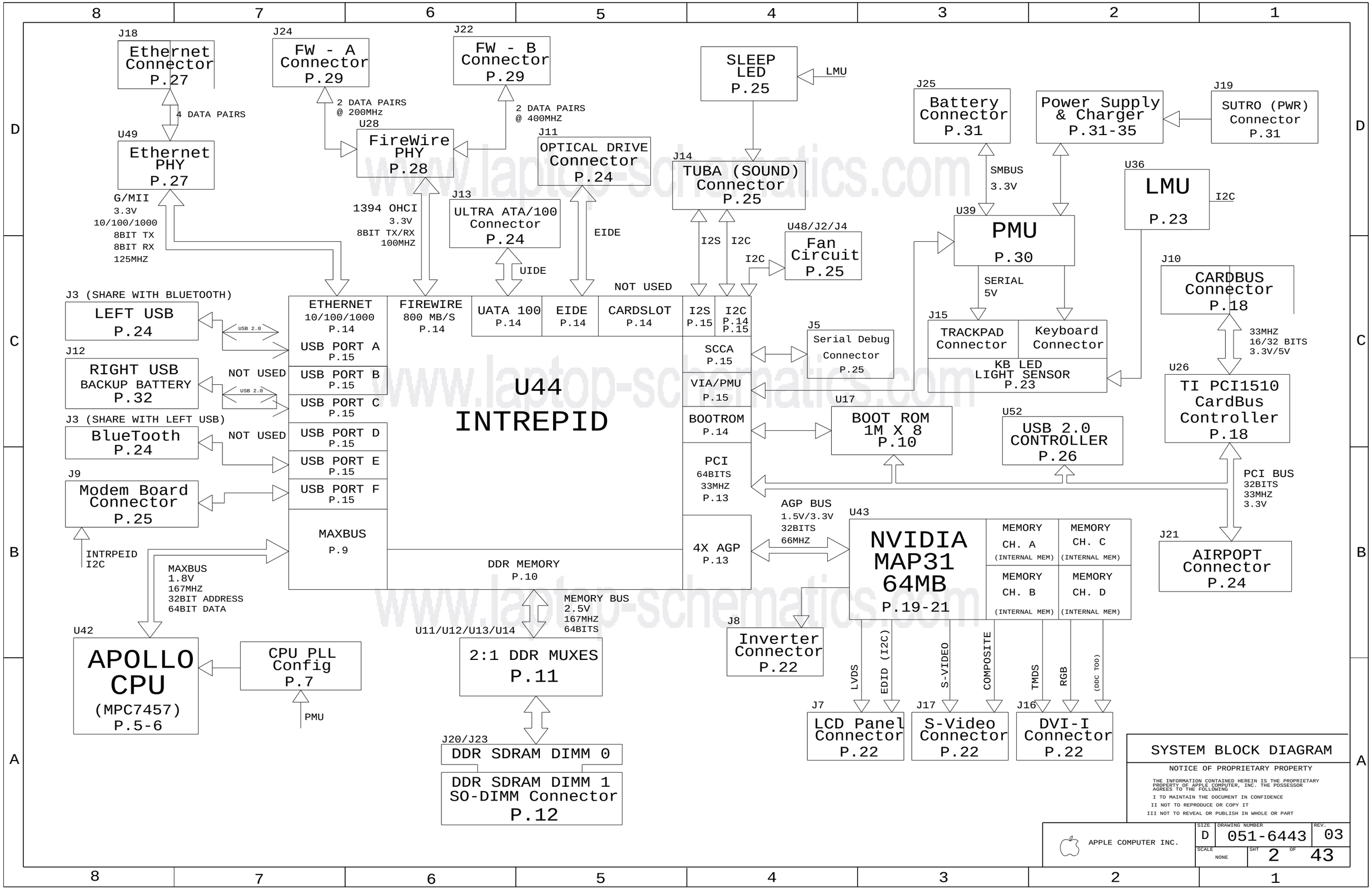

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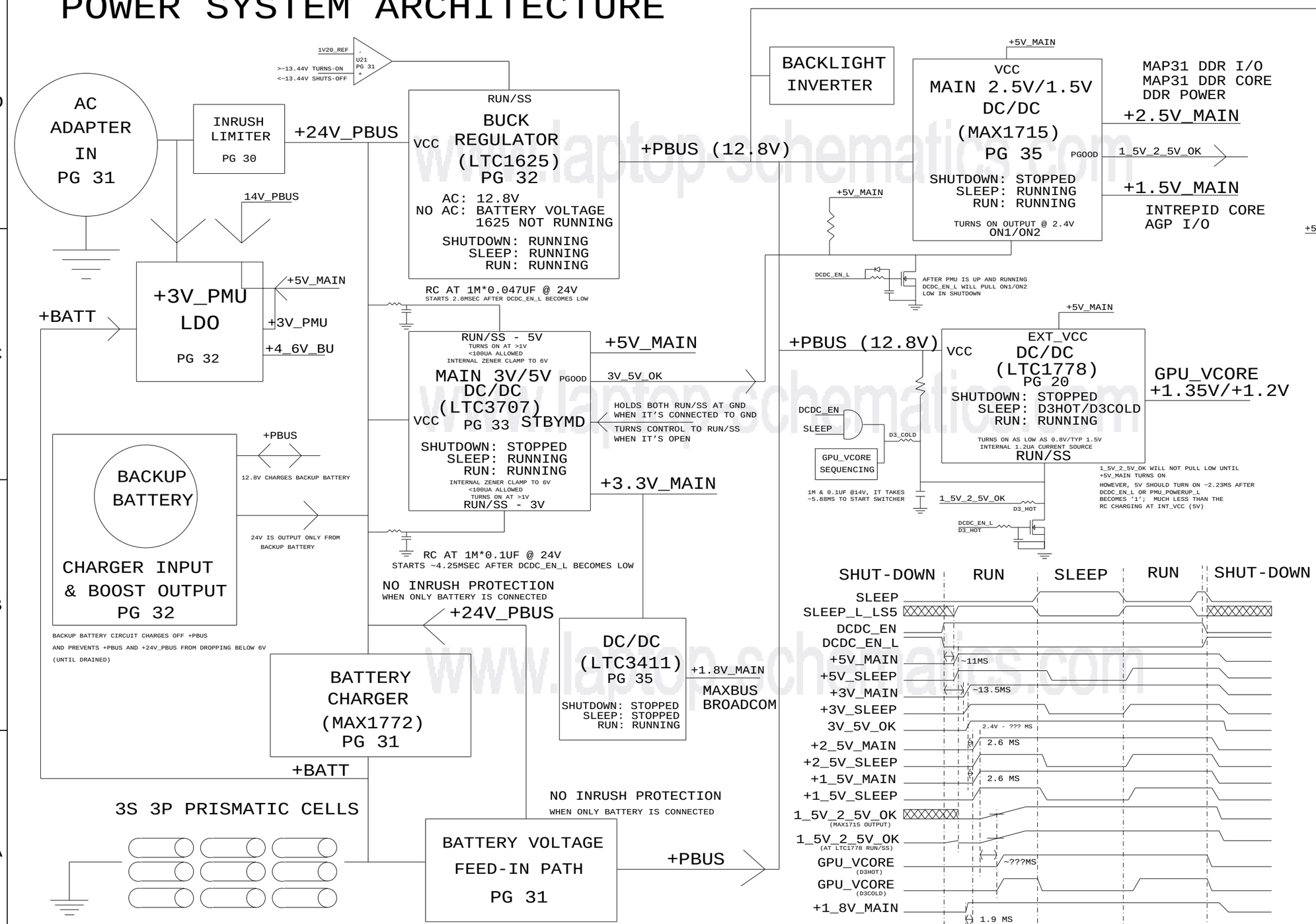
POWER SYSTEM ARCHITECTURE



POWER BLOCK DIAGRAM

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PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 12
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

20R10 TH VIA OR VIA IN PAD

1		SIGNAL (1/3 OZ + COPPER PLATING)
2	PREPREG (3MIL)	GROUND (1/2 OZ)
3	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
4	PREPREG (3MIL)	SIGNAL (1/2 OZ)
5	LAMINATE (4MIL)	GROUND (1/2 OZ)
6	PREPREG (2MIL)	CUT POWER PLANE(1 OZ)
7	LAMINATE (3MIL)	CUT POWER PLANE(1 OZ)
8	PREPREG (2MIL)	GROUND (1/2 OZ)
9	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
10	PREPREG (3MIL)	SIGNAL (1/2 OZ)
11	LAMINATE (4MIL)	GROUND (1/2 OZ)
12	PREPREG (3MIL)	SIGNAL (1/3 OZ + COPPER PLATING)

BOARD HOLES

ASICS HEATSINK MOUNTS

OMIT ZT10 255R158
OMIT ZT2 255R158
OMIT ZT11 255R158
OMIT ZT6 235R126
OMIT ZT16 235R126

CHASSIS MOUNTS

I/O AREA

OMIT ZT5 146R126 — CHGND5
BS1 STDOFF-2170DX150IDX35H-TH — CHGND1
OMIT ZT83 146R126 — CHGND6

INVERTER

SH1 OG-503040 SHLD-SM — CHGND2

CONDUCTIVE MOUNTS

OMIT ZT4 235R126

SPEAKER CLIPS

SP6 SPKR_CLIP_P84
SP1 SPKR_CLIP_P84
SP3 SPKR_CLIP_P84
SP5 SPKR_CLIP_P84
SP2 SPKR_CLIP_P84
SP4 SPKR_CLIP_P84

GROUND VIAS

ZT77 HOLE-VIA-20R10
ZT81 HOLE-VIA-20R10
ZT24 HOLE-VIA-20R10
ZT38 HOLE-VIA-20R10
ZT36 HOLE-VIA-20R10
ZT27 HOLE-VIA-20R10
ZT40 HOLE-VIA-20R10
ZT39 HOLE-VIA-20R10
ZT37 HOLE-VIA-20R10
ZT28 HOLE-VIA-20R10
ZT30 HOLE-VIA-20R10
ZT34 HOLE-VIA-20R10
ZT33 HOLE-VIA-20R10
ZT43 HOLE-VIA-20R10
ZT46 HOLE-VIA-20R10

ZT35 HOLE-VIA-20R10
ZT50 HOLE-VIA-20R10
ZT44 HOLE-VIA-20R10
ZT66 HOLE-VIA-20R10
ZT67 HOLE-VIA-20R10
ZT52 HOLE-VIA-20R10
ZT53 HOLE-VIA-20R10
ZT70 HOLE-VIA-20R10
ZT71 HOLE-VIA-20R10
ZT78 HOLE-VIA-20R10
ZT69 HOLE-VIA-20R10
ZT65 HOLE-VIA-20R10
ZT47 HOLE-VIA-20R10
ZT45 HOLE-VIA-20R10
ZT49 HOLE-VIA-20R10

ZT48 HOLE-VIA-20R10
ZT56 HOLE-VIA-20R10
ZT72 HOLE-VIA-20R10
ZT55 HOLE-VIA-20R10
ZT29 HOLE-VIA-20R10
ZT74 HOLE-VIA-20R10
ZT82 HOLE-VIA-20R10
ZT79 HOLE-VIA-20R10
ZT68 HOLE-VIA-20R10
ZT60 HOLE-VIA-20R10
ZT58 HOLE-VIA-20R10
ZT41 HOLE-VIA-20R10
ZT9 HOLE-VIA-20R10
ZT7 HOLE-VIA-20R10
ZT8 HOLE-VIA-20R10

ZT57 HOLE-VIA-20R10
ZT1 HOLE-VIA-20R10
ZT80 HOLE-VIA-20R10
ZT73 HOLE-VIA-20R10
ZT75 HOLE-VIA-20R10
ZT63 HOLE-VIA-20R10
ZT61 HOLE-VIA-20R10
ZT54 HOLE-VIA-20R10
ZT51 HOLE-VIA-20R10
ZT42 HOLE-VIA-20R10
ZT64 HOLE-VIA-20R10
ZT76 HOLE-VIA-20R10
ZT62 HOLE-VIA-20R10
ZT59 HOLE-VIA-20R10
ZT21 HOLE-VIA-20R10

ZT22 HOLE-VIA-20R10
ZT25 HOLE-VIA-20R10
ZT3 HOLE-VIA-20R10
ZT32 HOLE-VIA-20R10
ZT31 HOLE-VIA-20R10
ZT26 HOLE-VIA-20R10
ZT23 HOLE-VIA-20R10
ZT19 HOLE-VIA-20R10
ZT17 HOLE-VIA-20R10
ZT15 HOLE-VIA-20R10
ZT13 HOLE-VIA-20R10
ZT12 HOLE-VIA-20R10
ZT14 HOLE-VIA-20R10
ZT18 HOLE-VIA-20R10
ZT20 HOLE-VIA-20R10

BOARD INFORMATION

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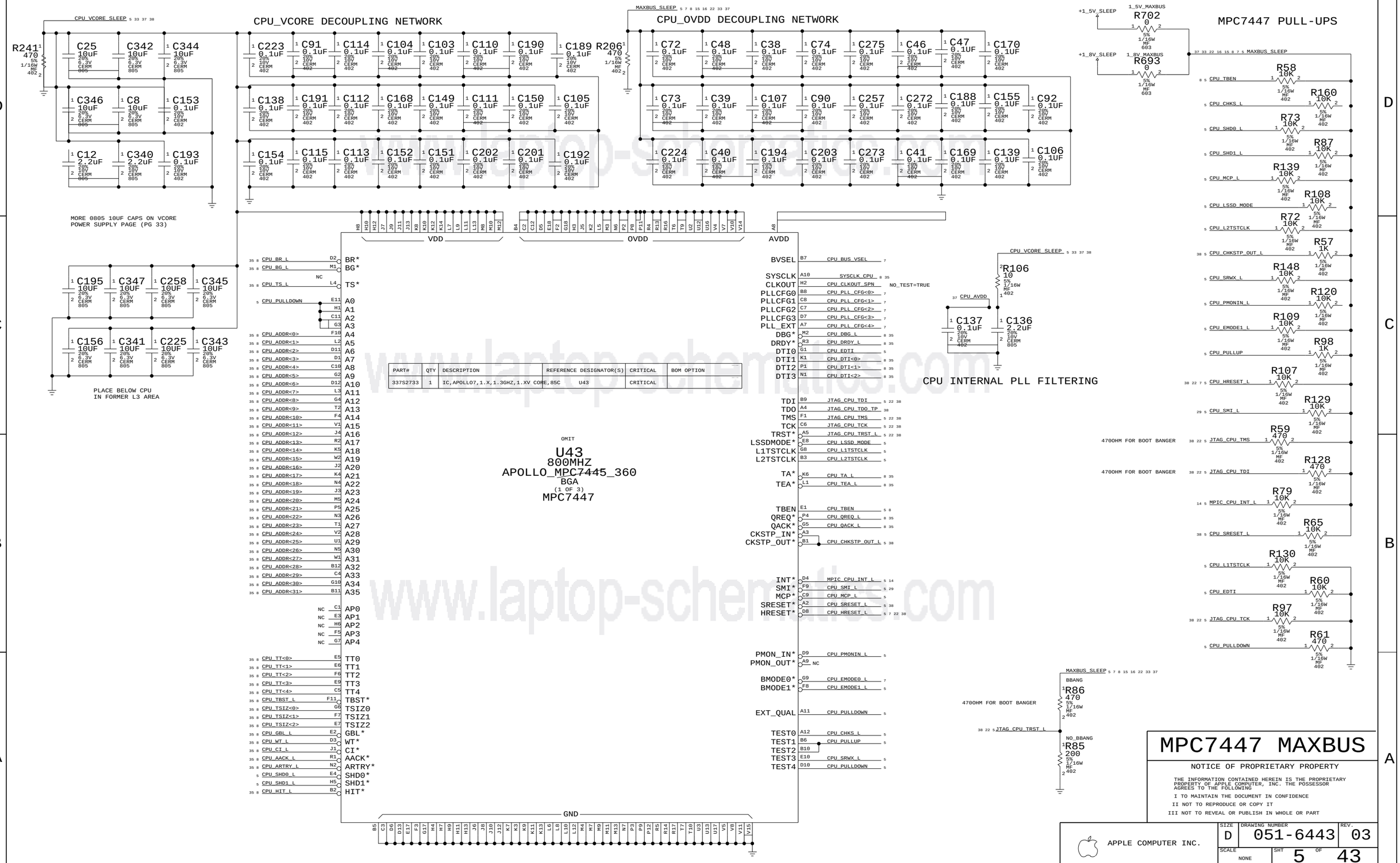

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S2733	1	IC,APOLLO7,1.X,1.3GHZ,1.XV CORE,85C	U43	CRITICAL	

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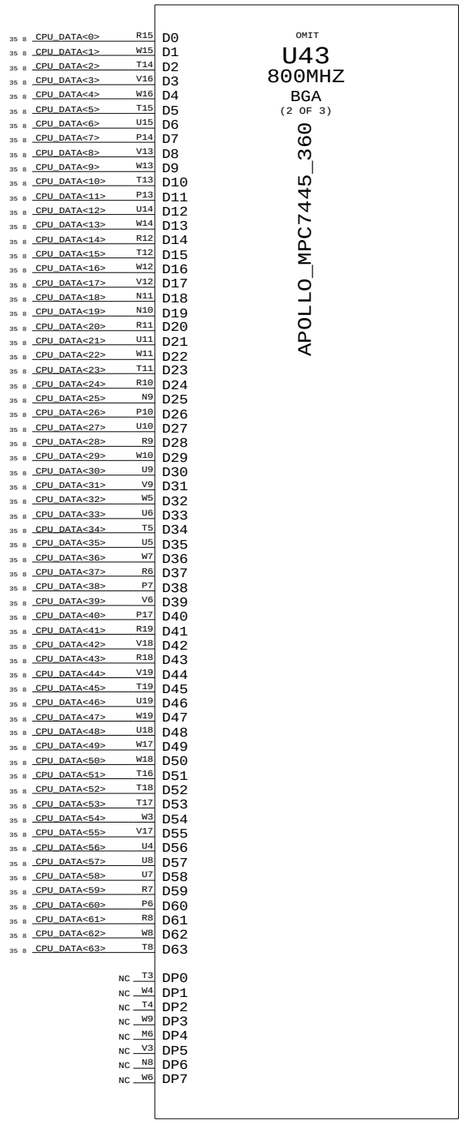
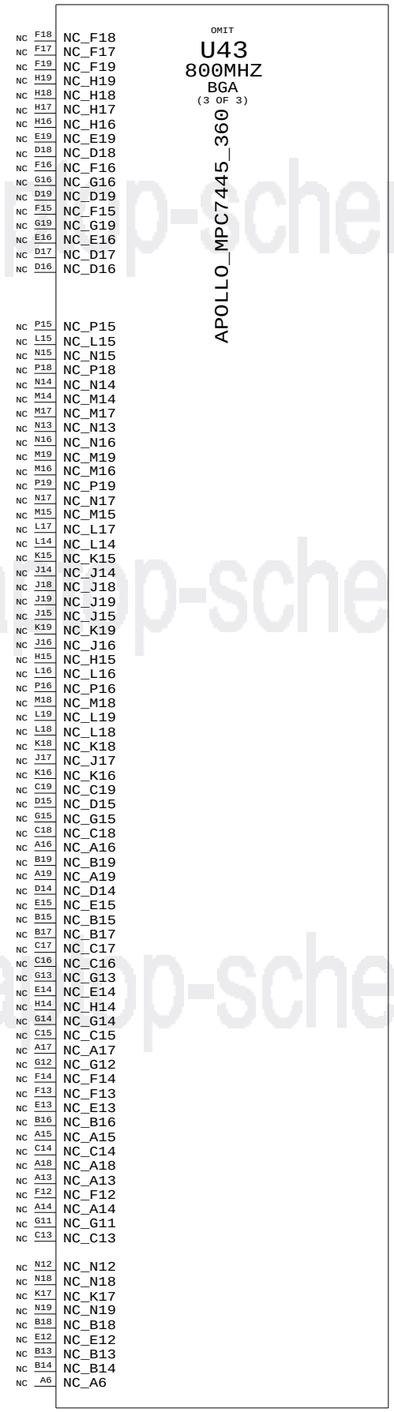
BOOT BANGER - LMU PERORMS THIS FUNCTION IF NEEDED
SEE PAGE 22





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MPC7447/BBANG

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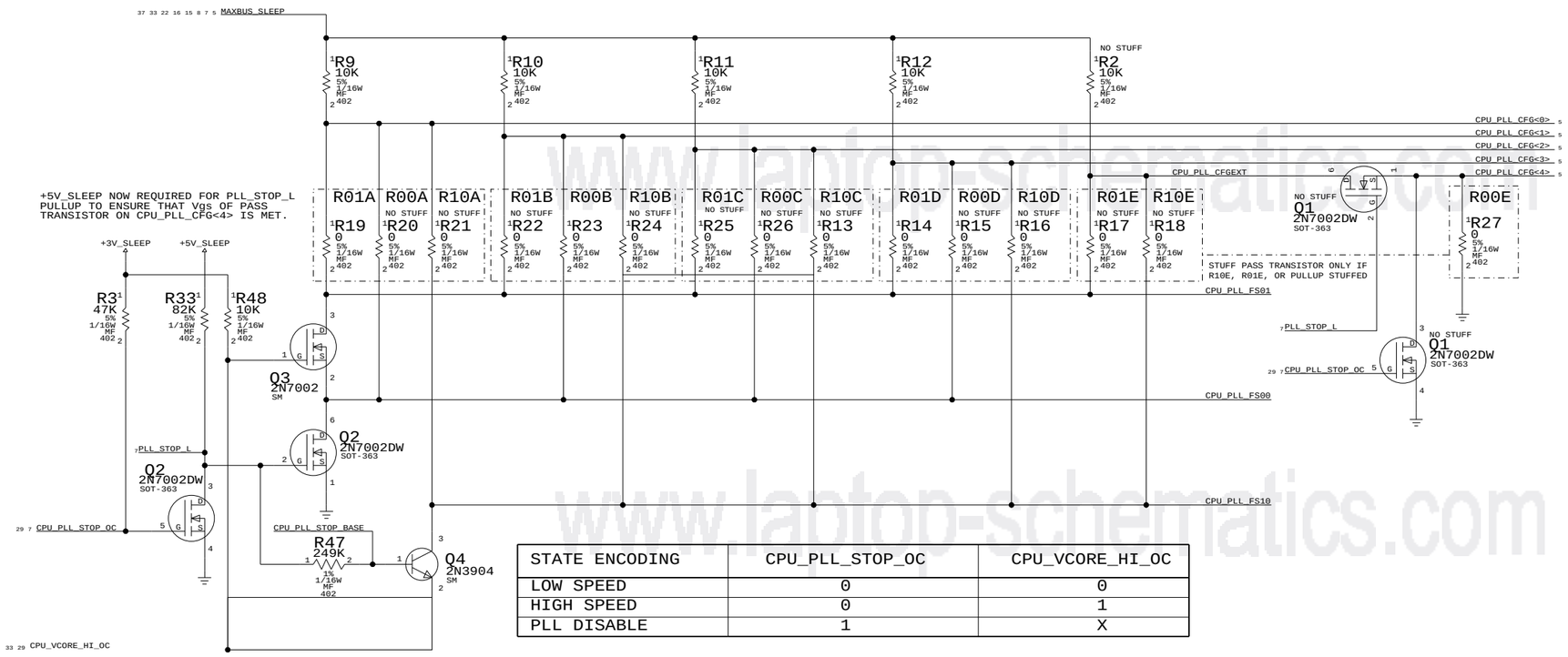
CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

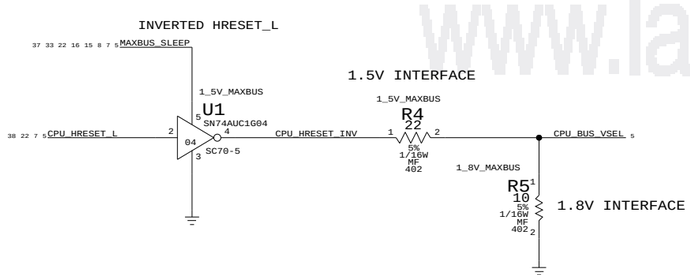
CPU FREQUENCY CONFIGURATION

APOLLO 7

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ (MHZ)	133MHZ (MHZ)	CPU_PLL_CFG 4 E	0123 ABCD	HEX
0.0X	PLL OFF		0	1111	0F
1.0X	PLL BYPASS		0	0011	03
2.0X	333	267	0	0100	04
3.0X	500	400	0	1000	08
4.0X	667	533	0	1010	0A
5.0X	833	667	0	1011	0B
5.5X	917	733	0	1001	09
6.0X	1000	800	0	1101	0D
6.5X	1083	867	0	0101	05
7.0X	1167	933	0	0010	02
7.5X	1250	1000	0	0001	01
8.0X	1333	1067	0	1100	0C
8.5X	1417	1133	0	0110	06
9.0X	1500	1200	1	0111	17
9.5X	1583	1267	0	0111	07
10.0X	1667	1333	1	1010	1A
10.5X	1750	1400	1	1000	18
11.0X	1833	1467	1	1001	19
11.5X	1917	1533	0	0000	00
12.0X	2000	1600	1	1011	1B
12.5X	2083	1667	1	1111	1F
13.0X	2167	1733	1	0101	15
13.5X	2250	1800	0	1110	0E
14.0X	2333	1867	1	1100	1C
15.0X	2500	2000	1	0001	11
16.0X	2667	2133	1	1101	1D
17.0X	2833	2267	1	0000	10
18.0X	3000	2400	1	0010	12
20.0X	3333	2667	1	0011	13
21.0X	3500	2800	1	0100	14
24.0X	4000	3200	1	0110	16
28.0X	4667	3733	1	1110	1E

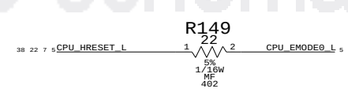
CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

BUSTYPE SELECT



APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION

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INTREPID BOOT STRAPS

BIT 32 TO 39

MAXBUS_SLEEP

Resistor	Net	Function
NO STUFF R642[1] 10K 5% 1/16W MF 402	CPU_DATA<32>	
NO STUFF R135[1] 10K 5% 1/16W MF 402	CPU_DATA<33>	
NO STUFF R123[1] 10K 5% 1/16W MF 402	CPU_DATA<34>	
NO STUFF R153[1] 10K 5% 1/16W MF 402	CPU_DATA<35>	
NO STUFF R166[1] 10K 5% 1/16W MF 402	CPU_DATA<36>	
NO STUFF R179[1] 10K 5% 1/16W MF 402	CPU_DATA<37>	
NO STUFF R651[1] 10K 5% 1/16W MF 402	CPU_DATA<38>	
NO STUFF R178[1] 10K 5% 1/16W MF 402	CPU_DATA<39>	
R136[1] 10K 5% 1/16W MF 402	DDR_TPWRDEFault_h 0: Tdi input 1: Tdi output	
R643[1] 10K 5% 1/16W MF 402	Analyzerclk_En_h 0: Inactive 1: Active	
R639[1] 10K 5% 1/16W MF 402	DDR_TPWRDEFault_h 0: Active high 1: Active low	
R657[1] 10K 5% 1/16W MF 402	ExtPLL_SDwn_Pol 0: Active high 1: Active low	
R664[1] 10K 5% 1/16W MF 402	Spare	
R673[1] 10K 5% 1/16W MF 402	Spare	
R143[1] 10K 5% 1/16W MF 402	Spare	
R674[1] 10K 5% 1/16W MF 402	Spare	

BIT 40 TO 47

MAXBUS_SLEEP

Resistor	Net	Function
NO STUFF R122[1] 10K 5% 1/16W MF 402	CPU_DATA<40>	
NO STUFF R142[1] 10K 5% 1/16W MF 402	CPU_DATA<41>	
NO STUFF R164[1] 10K 5% 1/16W MF 402	CPU_DATA<42>	
SSCG R134[1] 10K 5% 1/16W MF 402	CPU_DATA<43>	
NO STUFF R184[1] 10K 5% 1/16W MF 402	CPU_DATA<44>	
NO_SSCG R177[1] 10K 5% 1/16W MF 402	CPU_DATA<45>	
NO_SSCG R152[1] 10K 5% 1/16W MF 402	CPU_DATA<46>	
NO_SSCG R165[1] 10K 5% 1/16W MF 402	CPU_DATA<47>	
NO_SSCG R640[1] 10K 5% 1/16W MF 402	Spare	
NO_SSCG R652[1] 10K 5% 1/16W MF 402	Spare	
NO_SSCG R665[1] 10K 5% 1/16W MF 402	BIT2	
NO_SSCG R644[1] 10K 5% 1/16W MF 402	BIT1	
NO_SSCG R683[1] 10K 5% 1/16W MF 402	BIT0	
SSCG R675[1] 10K 5% 1/16W MF 402	InternalSpreadEn 1: Active	
SSCG R658[1] 10K 5% 1/16W MF 402	PCI1_Source Clock 0: PLL4 (NO SPREAD) 1: PLL6 (NO SPREAD)	
SSCG R666[1] 10K 5% 1/16W MF 402	PCI0_Source Clock 0: PLL5 (NO SPREAD)	

PLL4MODESEL_NXT[2:0]
000: 166.4MHZ (2.5X)
001: 149.76MHZ
010: 133.12MHZ (2.0X)
011: 99.84MHZ (1.5X)
100: 83.20MHZ

MODE A (2.5X) IS FOR STATIC OPERATION
MODE C (2.0X) IS FOR CLOCK SLEW OPERATION

BIT 48 TO 55

MAXBUS_SLEEP

Resistor	Net	Function
SSCG R133[1] 10K 5% 1/16W MF 402	CPU_DATA<48>	
SSCG R121[1] 10K 5% 1/16W MF 402	CPU_DATA<49>	
NO STUFF R163[1] 10K 5% 1/16W MF 402	CPU_DATA<50>	
NO STUFF R151[1] 10K 5% 1/16W MF 402	CPU_DATA<51>	
NO STUFF R162[1] 10K 5% 1/16W MF 402	CPU_DATA<52>	
NO STUFF R141[1] 10K 5% 1/16W MF 402	CPU_DATA<53>	
NO STUFF R183[1] 10K 5% 1/16W MF 402	CPU_DATA<54>	
NO STUFF R176[1] 10K 5% 1/16W MF 402	CPU_DATA<55>	
NO_SSCG R645[1] 10K 5% 1/16W MF 402	BUF_REF_CLK_OUTEnable_h 1: Active	
NO_SSCG R641[1] 10K 5% 1/16W MF 402	SetPLL4extSrc 1: External source	
NO STUFF R668[1] 10K 5% 1/16W MF 402	Spare	
NO STUFF R659[1] 10K 5% 1/16W MF 402	TI 1394b workaround 1: TI PHY workaround	
NO STUFF R667[1] 10K 5% 1/16W MF 402		
NO STUFF R653[1] 10K 5% 1/16W MF 402	BIT2	
NO STUFF R684[1] 10K 5% 1/16W MF 402	BIT1	
NO STUFF R676[1] 10K 5% 1/16W MF 402	BIT0	
		Spare

MaxBus output impedance
111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm

THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:
1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
2/ D46 - SELPCI1SPREADCLK - SLEEP/WAKE CYCLE REQUIRED
3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

IF A STRAP IS NOT LISTED, THEN IT CANNOT BE CHANGED BY SOFTWARE

R227 4.7 5% 1/16W MF 402
+1.5V_INTREPID_PLL — +1.5V_INTREPID_PLL7
C308 0.22UF 20% 6.3V CERM 402

U45 INTREPID-REV2.1 BGA (1 OF 9) CRITICAL
VDD15A_7 (PLL6) H26
VSSA_7 (PLL6) H25

Pin	Net	Function
E29	CPU_BR_L	BR INPUT
E26	CPU_BG_L	BG NO BUS KEEPER
B27	CPU_TS_L	TS NO BUS KEEPER
D24	CPU_ADDR<0>	A_0
D25	CPU_ADDR<1>	A_1
A27	CPU_ADDR<2>	A_2
E24	CPU_ADDR<3>	A_3
G23	CPU_ADDR<4>	A_4
B26	CPU_ADDR<5>	A_5
A26	CPU_ADDR<6>	A_6
D23	CPU_ADDR<7>	A_7
A25	CPU_ADDR<8>	A_8
E23	CPU_ADDR<9>	A_9
J22	CPU_ADDR<10>	A_10
B25	CPU_ADDR<11>	A_11
H22	CPU_ADDR<12>	A_12
G22	CPU_ADDR<13>	A_13
D22	CPU_ADDR<14>	A_14
B24	CPU_ADDR<15>	A_15
B23	CPU_ADDR<16>	A_16
E22	CPU_ADDR<17>	A_17
J21	CPU_ADDR<18>	A_18
G21	CPU_ADDR<19>	A_19
E21	CPU_ADDR<20>	A_20
A24	CPU_ADDR<21>	A_21
D21	CPU_ADDR<22>	A_22
A23	CPU_ADDR<23>	A_23
H20	CPU_ADDR<24>	A_24
B22	CPU_ADDR<25>	A_25
H21	CPU_ADDR<26>	A_26
A22	CPU_ADDR<27>	A_27
E20	CPU_ADDR<28>	A_28
B21	CPU_ADDR<29>	A_29
D20	CPU_ADDR<30>	A_30
A21	CPU_ADDR<31>	A_31
G26	CPU_CI_L	CI
A29	CPU_GBL_L	GBL
A28	CPU_TBST_L	TBST
G24	CPU_TSIZ<0>	TSIZ_0
H24	CPU_TSIZ<1>	TSIZ_1
D26	CPU_TSIZ<2>	TSIZ_2
E25	CPU_TT<0>	TT_0
G25	CPU_TT<1>	TT_1
B28	CPU_TT<2>	TT_2
D27	CPU_TT<3>	TT_3
J25	CPU_TT<4>	TT_4
D28	CPU_WT_L	WT
B29	CPU_AACK_L	AACK NO BUS KEEPER - PU
H23	CPU_ARTRY_L	ARTRY NO BUS KEEPER - PU
B31	CPU_HIT_L	HIT INPUT - PU
A32	CPU_QREQ_L	QREQ INPUT - PD
G27	CPU_QACK_L	QACK NO BUS KEEPER - ?
AK9	INT_SUSPEND_REQ_L	SUSPENDREQ
AM8	INT_SUSPEND_ACK_L	SUSPENDACK
J24	INT_CPUFB_IN	CPU_FB_IN
H16	INT_CPUFB_OUT	CPU_FB_OUT NO BUS KEEPER - PU
G8	SYSCLK_LA_TP	ANALYZER_CLK
AH9	CPU_CLK_EN	STOPCPUCLK INPUT - PU
H13	INTREPID_ACS_REF	ACS_REF NO BUS KEEPER - ?
J15	SYSCLK_CPU_UF	CPU_CLK NO BUS KEEPER - PU
A31	CPU_TBEN	TBEN NO BUS KEEPER - PU
D10	CPU_DATA<0>	D_0
G12	CPU_DATA<1>	D_1
E11	CPU_DATA<2>	D_2
H11	CPU_DATA<3>	D_3
B9	CPU_DATA<4>	D_4
B8	CPU_DATA<5>	D_5
A9	CPU_DATA<6>	D_6
A8	CPU_DATA<7>	D_7
E12	CPU_DATA<8>	D_8
D11	CPU_DATA<9>	D_9
B10	CPU_DATA<10>	D_10
J13	CPU_DATA<11>	D_11
A10	CPU_DATA<12>	D_12
D12	CPU_DATA<13>	D_13
E13	CPU_DATA<14>	D_14
G13	CPU_DATA<15>	D_15
B11	CPU_DATA<16>	D_16
D13	CPU_DATA<17>	D_17
A11	CPU_DATA<18>	D_18
G14	CPU_DATA<19>	D_19
H14	CPU_DATA<20>	D_20
E14	CPU_DATA<21>	D_21
B12	CPU_DATA<22>	D_22
G15	CPU_DATA<23>	D_23
B13	CPU_DATA<24>	D_24
H15	CPU_DATA<25>	D_25
D14	CPU_DATA<26>	D_26
B14	CPU_DATA<27>	D_27
A12	CPU_DATA<28>	D_28
G16	CPU_DATA<29>	D_29
E15	CPU_DATA<30>	D_30
J16	CPU_DATA<31>	D_31
D15	CPU_DATA<32>	D_32
A14	CPU_DATA<33>	D_33
A13	CPU_DATA<34>	D_34
D16	CPU_DATA<35>	D_35
E16	CPU_DATA<36>	D_36
G17	CPU_DATA<37>	D_37
B15	CPU_DATA<38>	D_38
H17	CPU_DATA<39>	D_39
A15	CPU_DATA<40>	D_40
B16	CPU_DATA<41>	D_41
E17	CPU_DATA<42>	D_42
A16	CPU_DATA<43>	D_43
J18	CPU_DATA<44>	D_44
H18	CPU_DATA<45>	D_45
D17	CPU_DATA<46>	D_46
G18	CPU_DATA<47>	D_47
A17	CPU_DATA<48>	D_48
B17	CPU_DATA<49>	D_49
E18	CPU_DATA<50>	D_50
B18	CPU_DATA<51>	D_51
D18	CPU_DATA<52>	D_52
A18	CPU_DATA<53>	D_53
A19	CPU_DATA<54>	D_54
H19	CPU_DATA<55>	D_55
B19	CPU_DATA<56>	D_56
J19	CPU_DATA<57>	D_57
A20	CPU_DATA<58>	D_58
D19	CPU_DATA<59>	D_59
E19	CPU_DATA<60>	D_60
G19	CPU_DATA<61>	D_61
B20	CPU_DATA<62>	D_62
G20	CPU_DATA<63>	D_63
A30	CPU_DBG_L	DBG
G28	CPU_DRDY_L	DRDY
K25	CPU_DTI<0>	DTI_0
D29	CPU_DTI<1>	DTI_1
B30	CPU_DTI<2>	DTI_2
E27	CPU_TA_L	TA
E28	CPU_TEA_L	TEA

Vin = Intrepid Vcore (1.5V)
Vout = MaxBus rail (1.8V)

MAXBUS INTERFACE

INTREPID OUTPUTS HIGH BY DEFAULT

FB BUFFER HAS 50 OHM OUTPUT IMPEDANCE

R197[1] 511 1% 1/16W MF 402
R144 0 5% 1/16W MF 402 — SYSCLK_CPU
R137[1] 1K 1% 1/16W MF 402

SHORT = 1" SHORTER THAN MATCHED LENGTH
LONG = 1" LONGER THAN MATCHED LENGTH

R167 0 5% 1/16W MF 402 — INT_CPUFB_OUT — INT_CPUFB_OUT_SHORT
R215 0 5% 1/16W MF 402 — INT_CPUFB_OUT_NORM
NO STUFF R207 0 5% 1/16W MF 402 — INT_CPUFB_LONG
NO STUFF R225[1] 0 5% 1/16W MF 402
R208[1] 0 5% 1/16W MF 402
R226 0 5% 1/16W MF 402 — INT_CPUFB_IN — INT_CPUFB_IN_NORM
NO STUFF R196 0 5% 1/16W MF 402

MAXBUS PULL-UPS

MAXBUS_SLEEP

Resistor	Net
RP21 10K 5% 1/16W SM1	CPU_TS_L
RP21 10K 5% 1/16W SM1	CPU_TA_L
RP21 10K 5% 1/16W SM1	CPU_ARTRY_L
RP23 10K 5% 1/16W SM1	CPU_BR_L
RP24 10K 5% 1/16W SM1	CPU_HIT_L
RP23 10K 5% 1/16W SM1	CPU_DRDY_L
RP23 10K 5% 1/16W SM1	CPU_TEA_L
RP23 10K 5% 1/16W SM1	CPU_AACK_L
RP24 10K 5% 1/16W SM1	CPU_DBG_L
RP21 10K 5% 1/16W SM1	CPU_BG_L
RP24 10K 5% 1/16W SM1	CPU_QREQ_L

INTREPID BOOT STRAPS

BIT 56 TO 63

MAXBUS_SLEEP

Resistor	Net	Function
NO STUFF R140[1] 10K 5% 1/16W MF 402	CPU_DATA<56>	
NO STUFF R161[1] 10K 5% 1/16W MF 402	CPU_DATA<57>	
NO STUFF R175[1] 10K 5% 1/16W MF 402	CPU_DATA<58>	
NO STUFF R132[1] 10K 5% 1/16W MF 402	CPU_DATA<59>	
NO STUFF R131[1] 10K 5% 1/16W MF 402	CPU_DATA<60>	
NO STUFF R150[1] 10K 5% 1/16W MF 402	CPU_DATA<61>	
NO STUFF R174[1] 10K 5% 1/16W MF 402	CPU_DATA<62>	
NO STUFF R182[1] 10K 5% 1/16W MF 402	CPU_DATA<63>	
R654[1] 10K 5% 1/16W MF 402	Spare	
R669[1] 10K 5% 1/16W MF 402	Spare	
R677[1] 10K 5% 1/16W MF 402	Spare	
R646[1] 10K 5% 1/16W MF 402	PCI1_REQ2_L 0: GPIO2 1: GNT2_L	
R647[1] 10K 5% 1/16W MF 402	PCI1_REQ1_L 0: GPIO1 1: GNT1_L	
R660[1] 10K 5% 1/16W MF 402	PCI1_REQ0_L 0: GPIO0 1: GNT0_L	
NO STUFF R678[1] 10K 5% 1/16W MF 402	Fireport PHY interface 0: Legacy interface 1: B-mode interface	
R685[1] 10K 5% 1/16W MF 402	Processor Bus Mode 0: 60x bus (32) 1: 60x bus (64)	

Intrepid MaxBus

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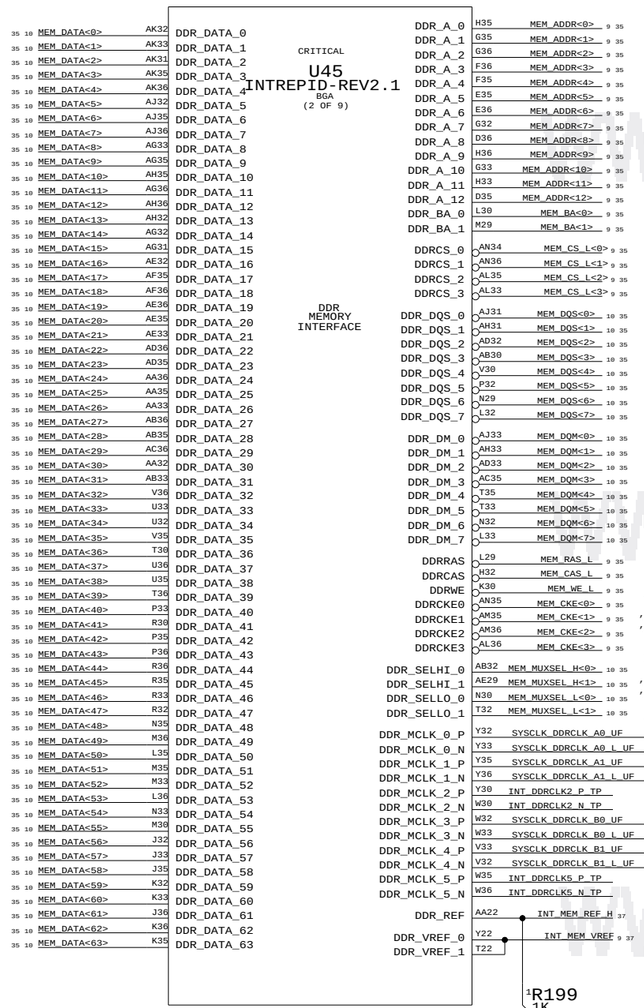
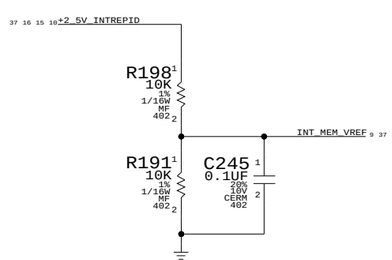
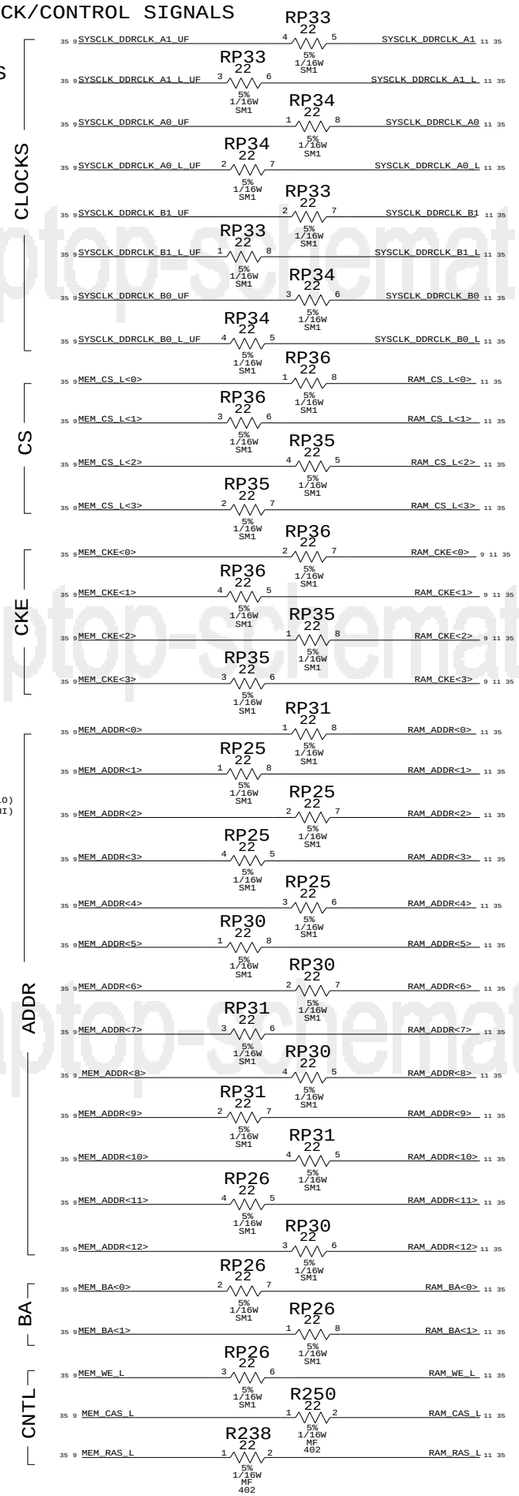
SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

PINS ARE SWAPABLE FOR RPAKS

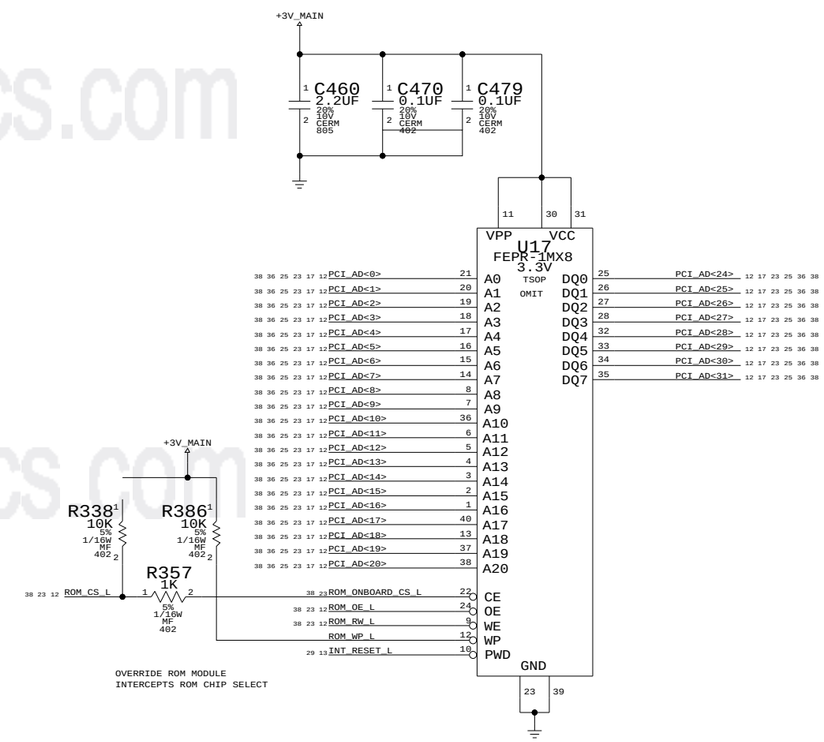


MEM_VREF



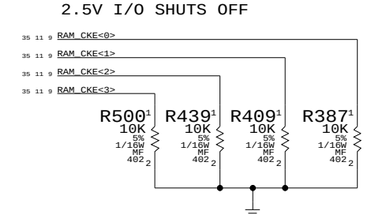


1MB BOOT ROM



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1193	1	BOOTROM,P84	U17	CRITICAL	?

PULL-DOWN RESISTORS TO ENSURE
CKE STAYS LOW AFTER INTREPID
2.5V I/O SHUTS OFF



INT - DDR/BOOTROM

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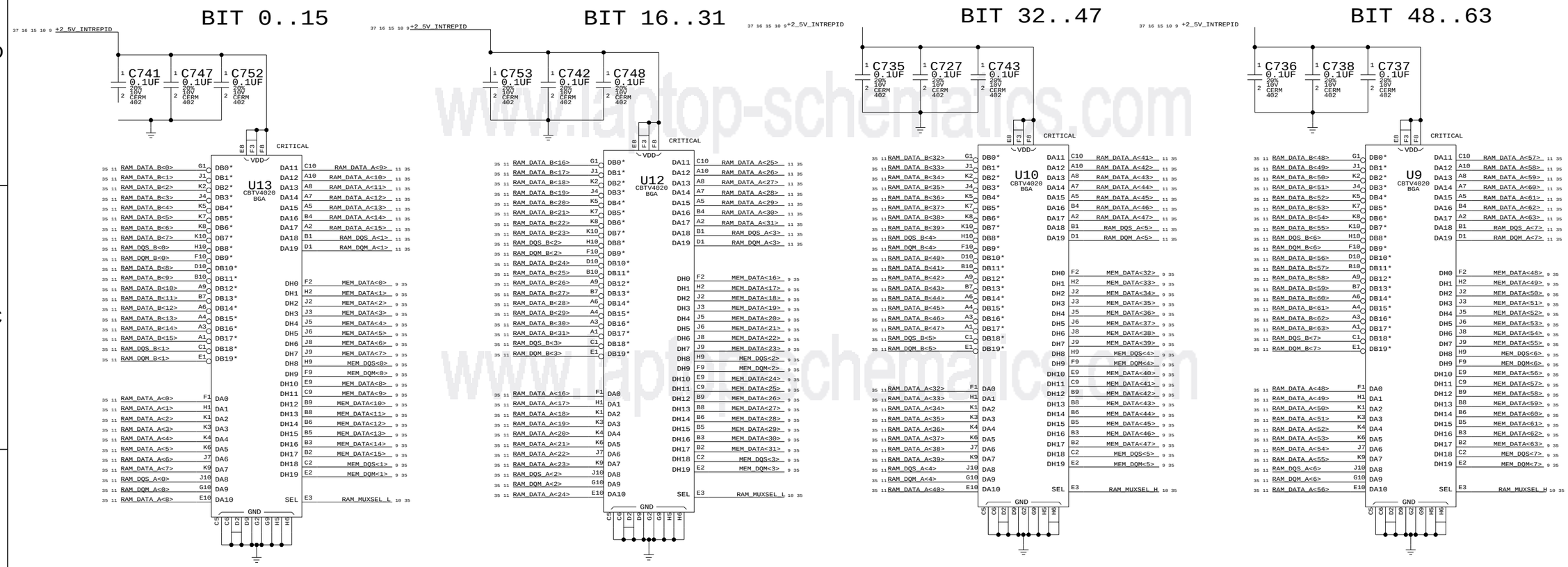

SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND
MEM_MUXSEL_H<0> AND MEM_MUXSEL_L<0> ARE ACTIVE LOW
MEM_MUXSEL_H<1> AND MEM_MUXSEL_L<1> ARE ACTIVE HIGH

ADDED 0 OHM RESISTORS IN CASE POLARITY IS WRONG

16BIT 2:1 DDR MUXES

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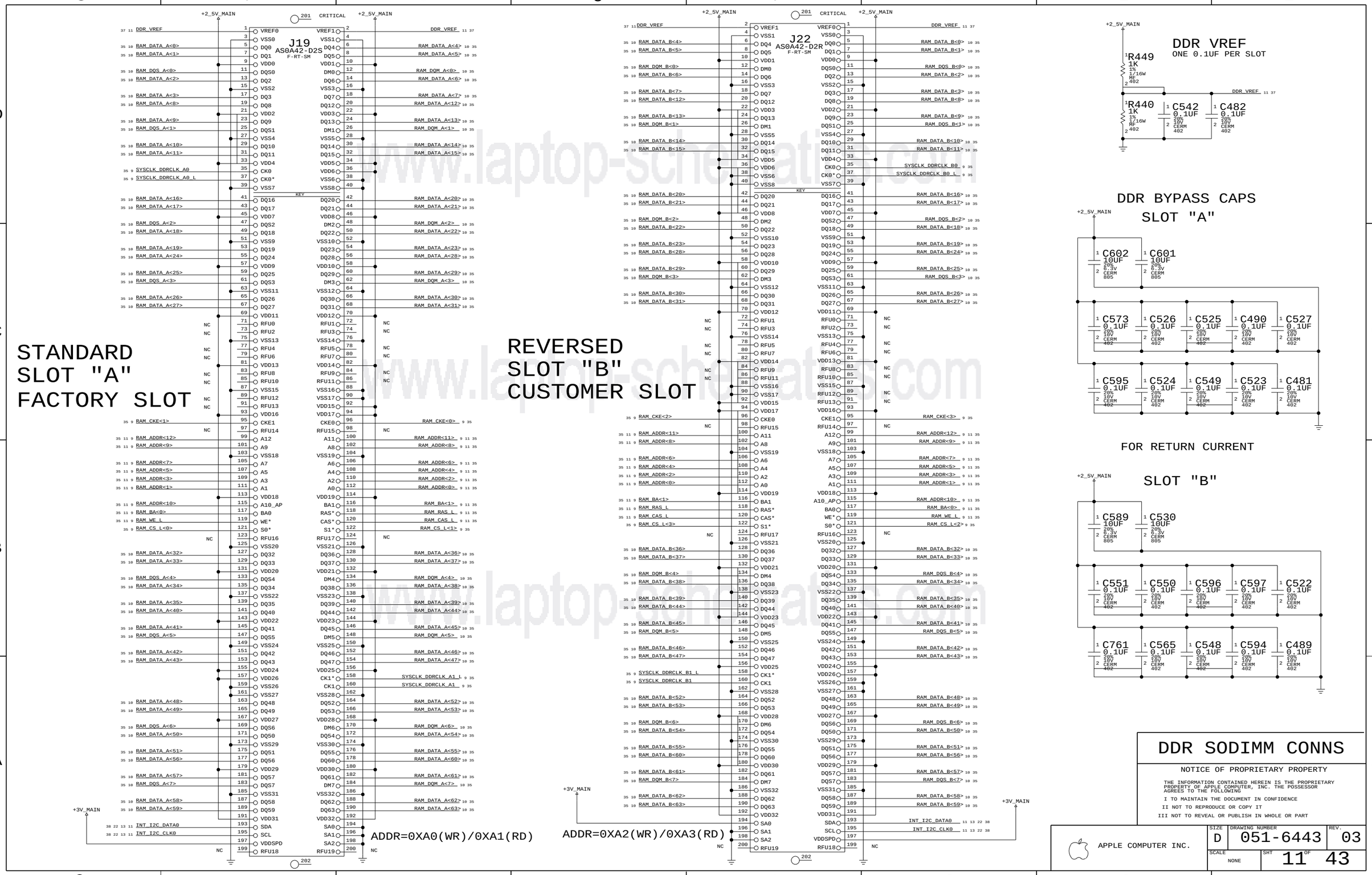
STANDARD
SLOT "A"
FACTORY SLOT
J19
AS0A42-D2S
F-RT-SM
REVERSED
SLOT "B"
CUSTOMER SLOT
J22
AS0A42-D2R
F-RT-SM
ADDR=0XA0(WR)/0XA1(RD)
ADDR=0XA2(WR)/0XA3(RD)
DDR VREF
ONE 0.1UF PER SLOT
DDR BYPASS CAPS
SLOT "A"
FOR RETURN CURRENT
SLOT "B"
DDR SODIMM CONNS
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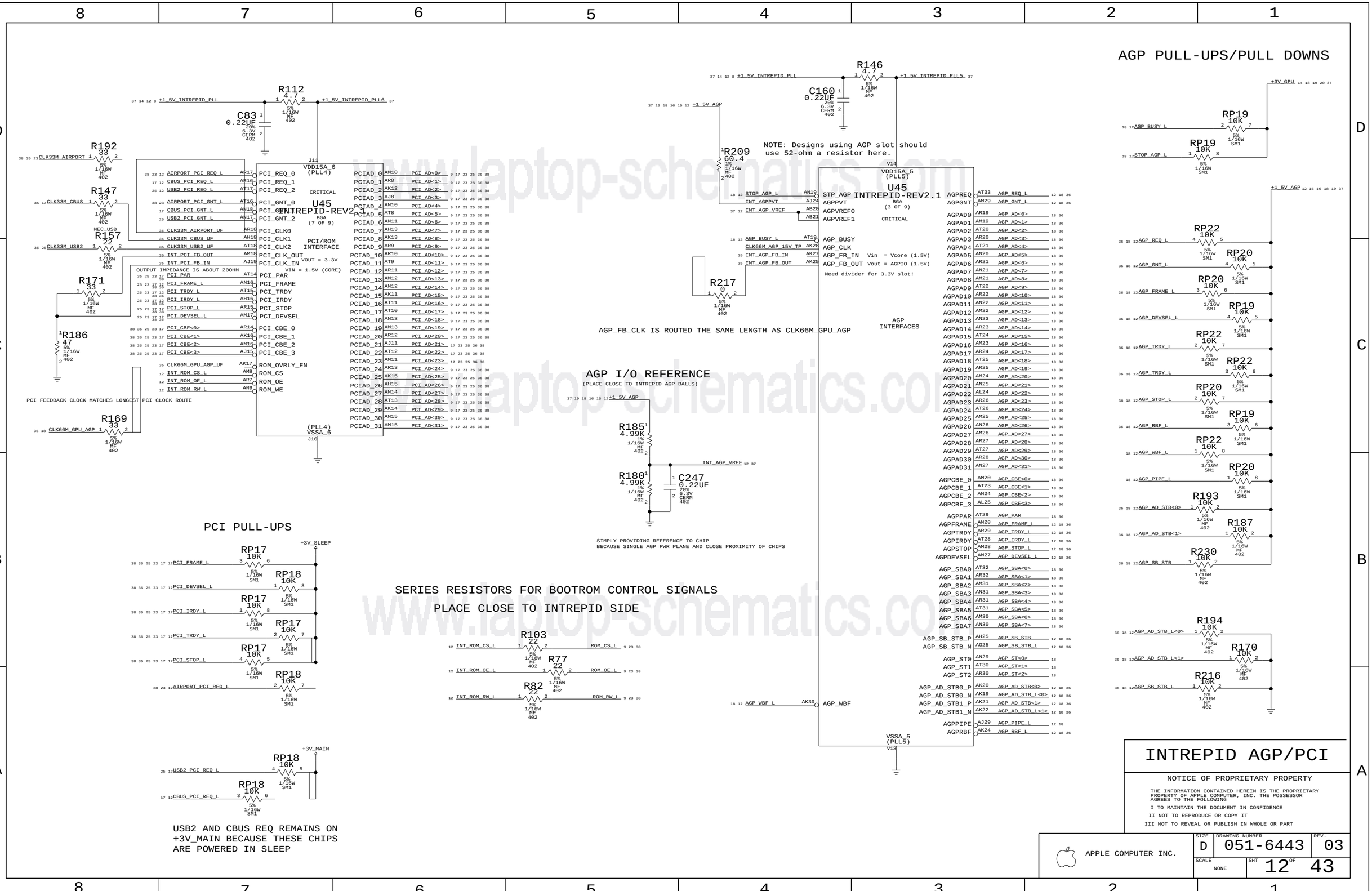
AGP PULL-UPS/PULL DOWNS
PCI PULL-UPS
AGP I/O REFERENCE
(PLACE CLOSE TO INTREPID AGP BALLS)
SIMPLY PROVIDING REFERENCE TO CHIP
BECAUSE SINGLE AGP PWR PLANE AND CLOSE PROXIMITY OF CHIPS
SERIES RESISTORS FOR BOOTROM CONTROL SIGNALS
PLACE CLOSE TO INTREPID SIDE
NOTE: Designs using AGP slot should
use 52-ohm a resistor here.
AGP_FB_CLK IS ROUTED THE SAME LENGTH AS CLK66M_GPU_AGP
PCI FEEDBACK CLOCK MATCHES LONGEST PCI CLOCK ROUTE
OUTPUT IMPEDANCE IS ABOUT 200HM
USB2 AND CBUS REQ REMAINS ON
+3V_MAIN BECAUSE THESE CHIPS
ARE POWERED IN SLEEP
U45
INTREPID-REV2.1
BGA
(7 OF 9)
PCI/ROM
INTERFACE
CRITICAL
VDD15A_6
(PLL4)
VSSA_6
(PLL4)
VOUT = 3.3V
VIN = 1.5V (CORE)
VDD15A_5
(PLL5)
VSSA_5
(PLL5)
(3 OF 9)
AGP
INTERFACES
Vin = Vcore (1.5V)
Vout = AGPIO (1.5V)
Need divider for 3.3V slot!
INTREPID AGP/PCI
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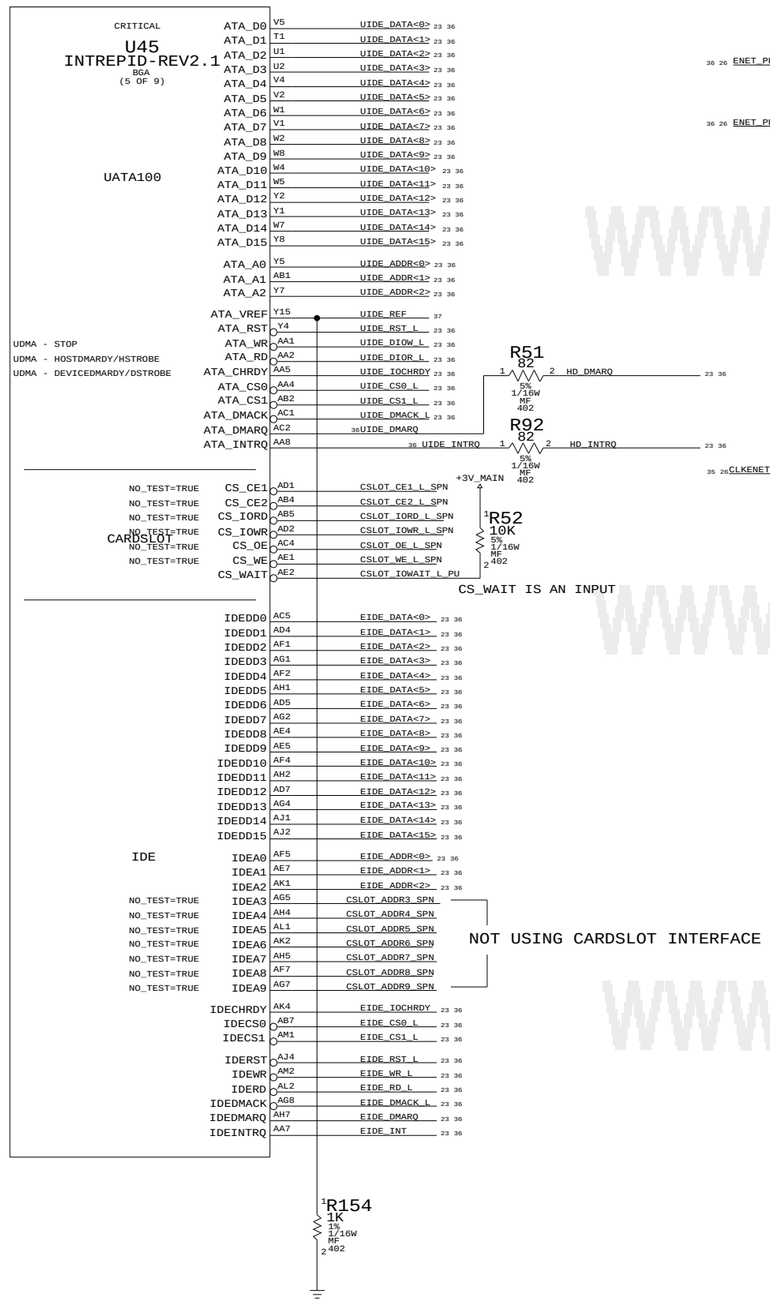
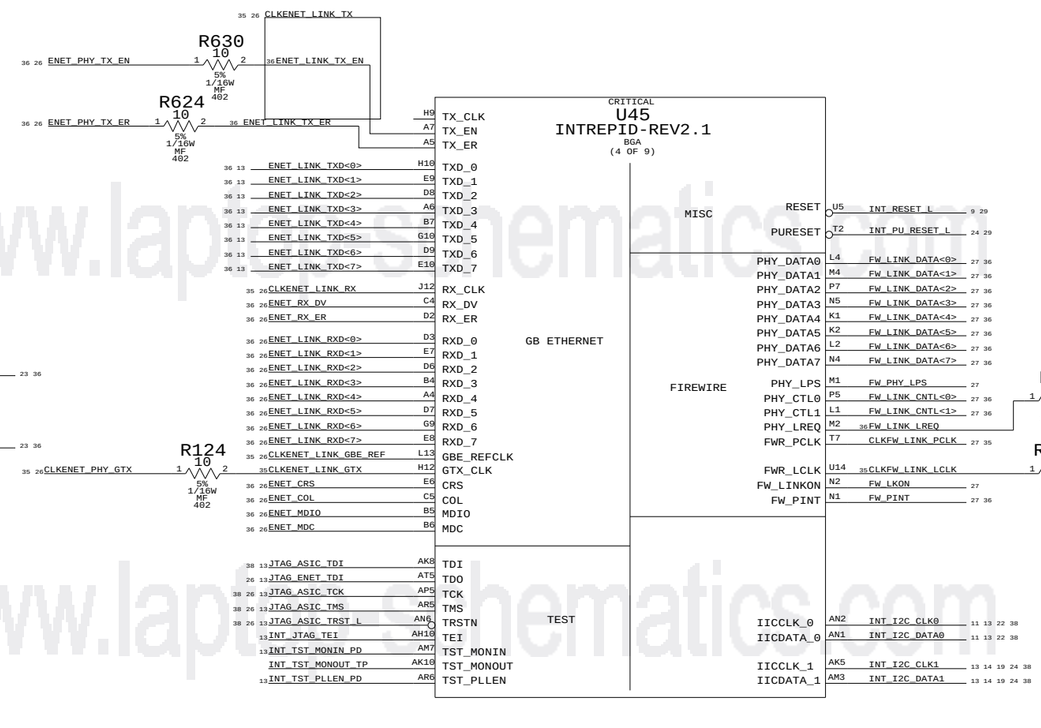
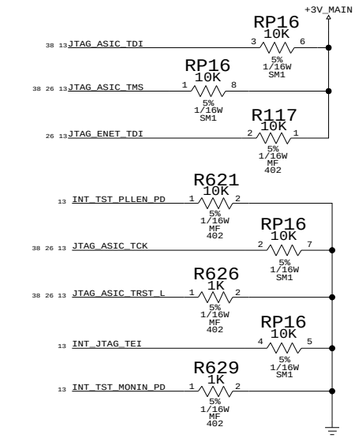
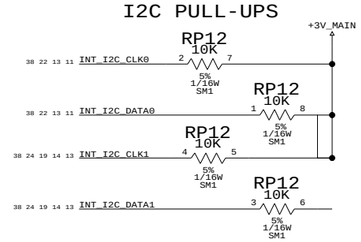




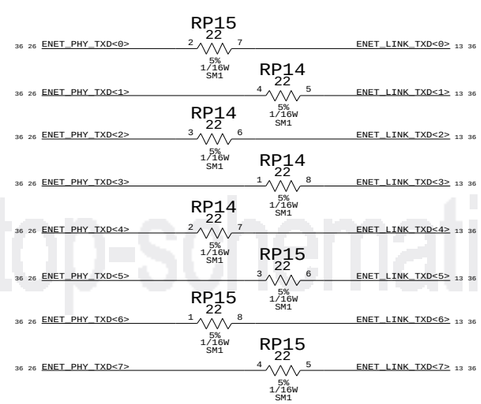
TEST PULL-UPS/DOWNS



I2C PULL-UPS



ENET_TXD SERIES TERMINATION



ADDR \ BUS	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR A1-RD	RAM - STANDARD J20 - PG 12	N/A	N/A	N/A
A2-WR A3-RD	RAM - REVERSED J23 - PG 12	N/A	N/A	N/A
AC-WR AD-RD	N/A	N/A	DASH MODEM J9 - PG 25	N/A
AE-WR AF-RD	BOOTBANG E2PROM U37 - PG 23	N/A	N/A	N/A
84-WR 85-RD	LMU U36 - PG 23	N/A	N/A	N/A
58-WR 59-RD	N/A	FAN CONTROLLER U48 - PG 25	N/A	N/A
6A-WR 6B-RD	N/A	N/A	SNAPPER SOUND J14 - PG 25	N/A
D0-WR D1-RD	N/A	CLOCK SLEW SSCG U56 - PG 15	N/A	N/A

ADDR LSB INDICATES READ ('1') OR WRITE ('0') MODES

JTG_RSTN_L	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR_ TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL_ TESTSEL5 (INPUT)	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

INT - ENET/FW/UATA EIDE/I2C

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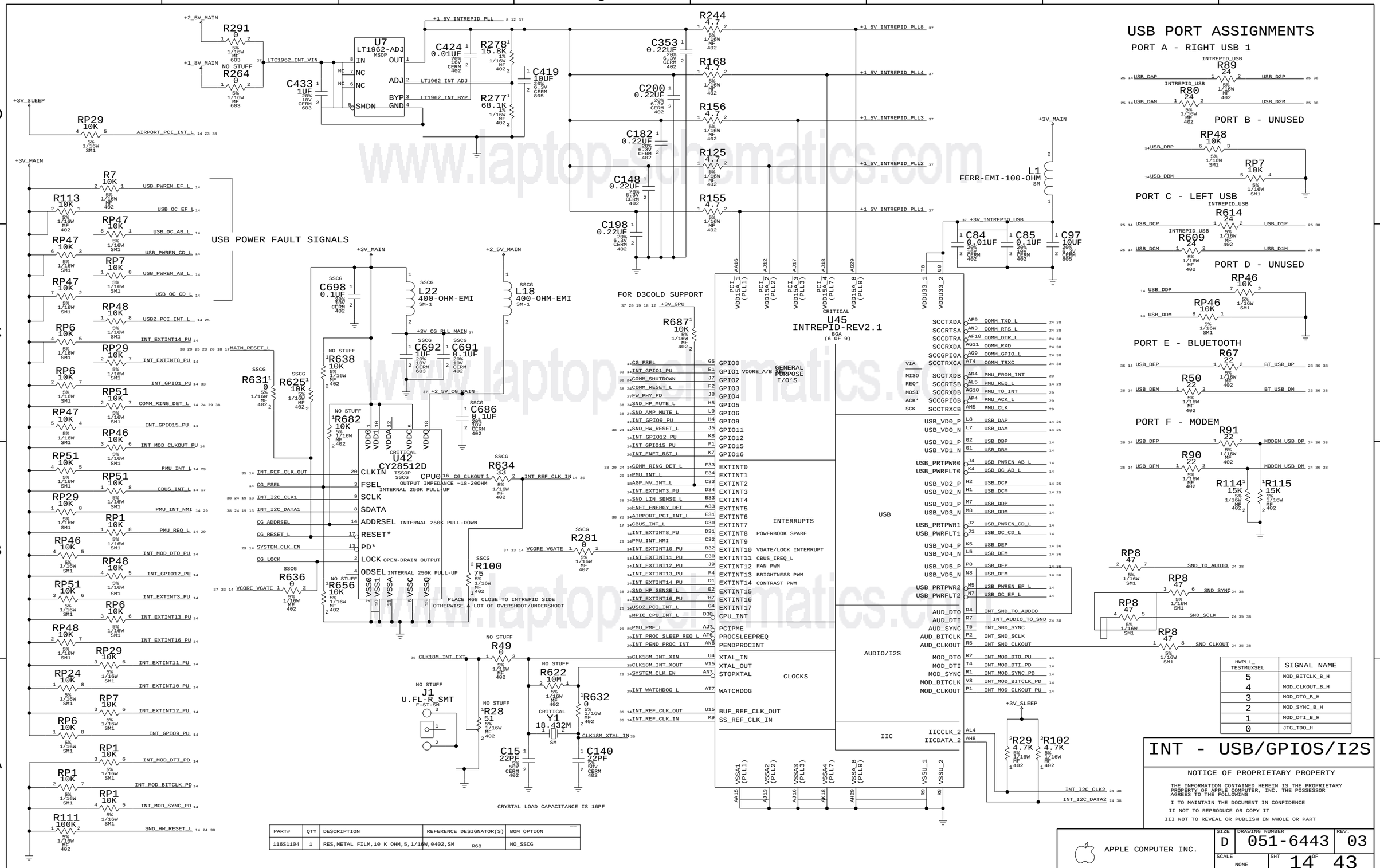

HWPLL_TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES,METAL FILM,10 K OHM,5,1/16W,0402,SM	R68	NO_SSCG

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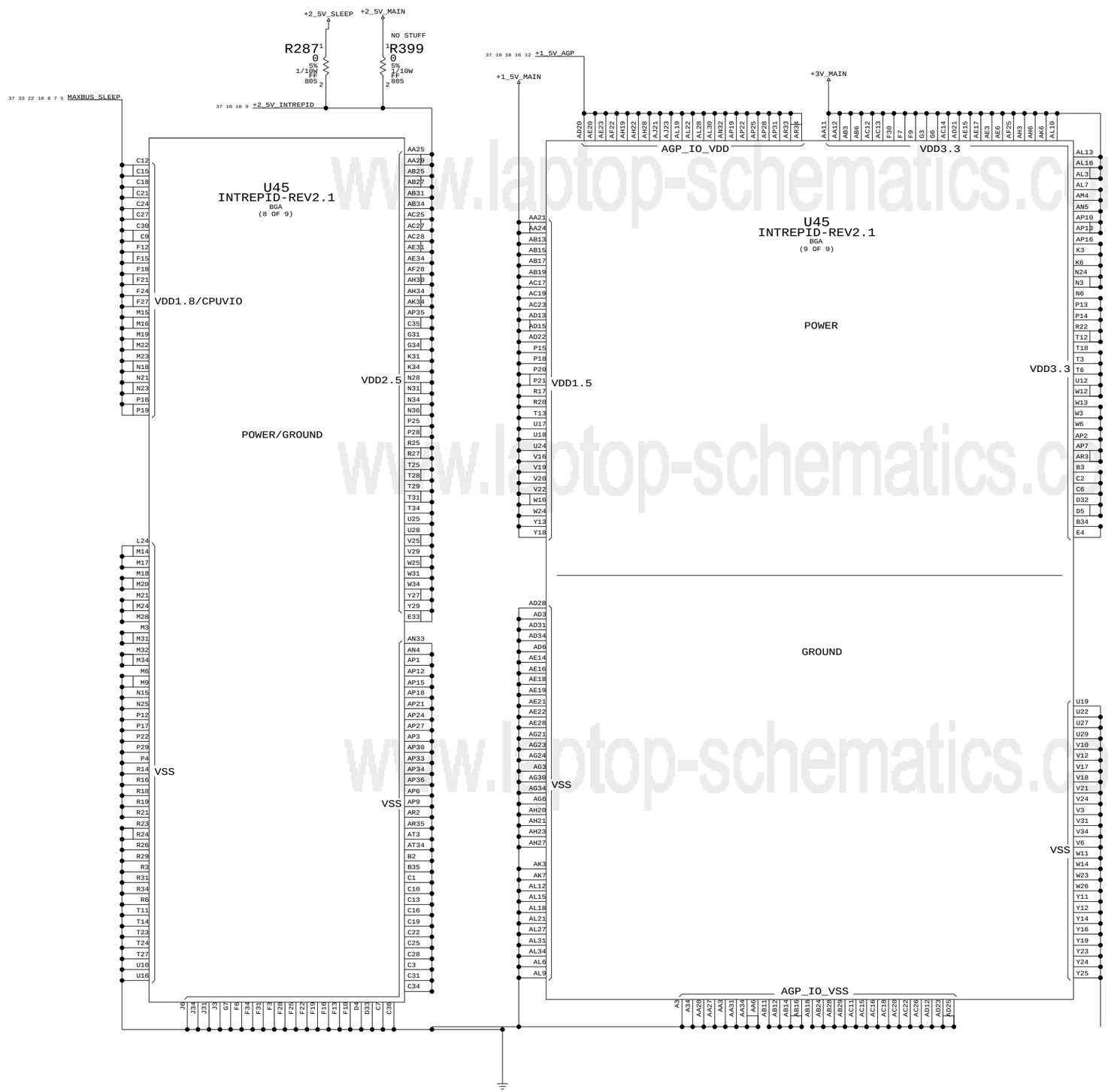

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Intrepid Power

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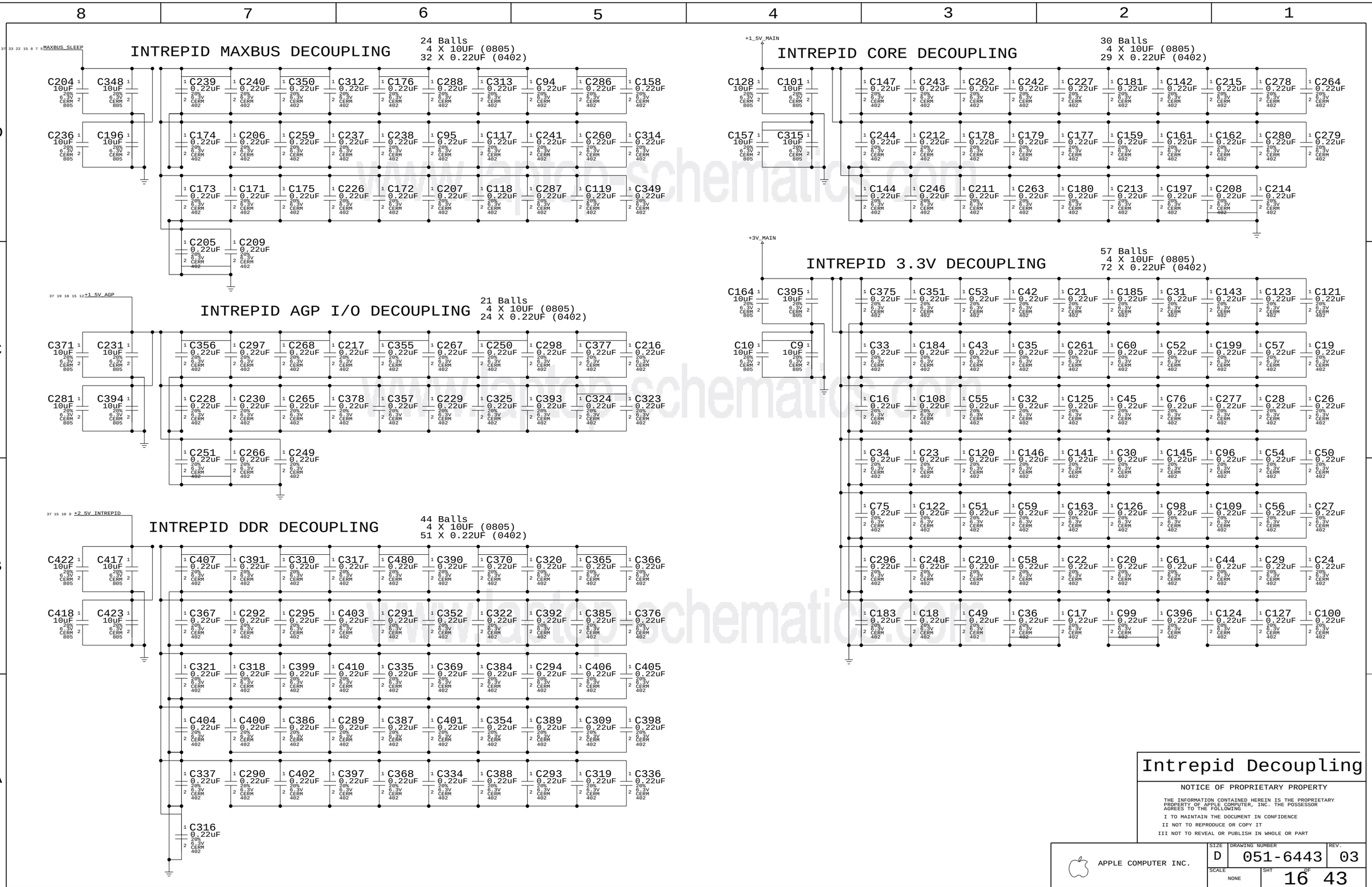

Intrepid Decoupling

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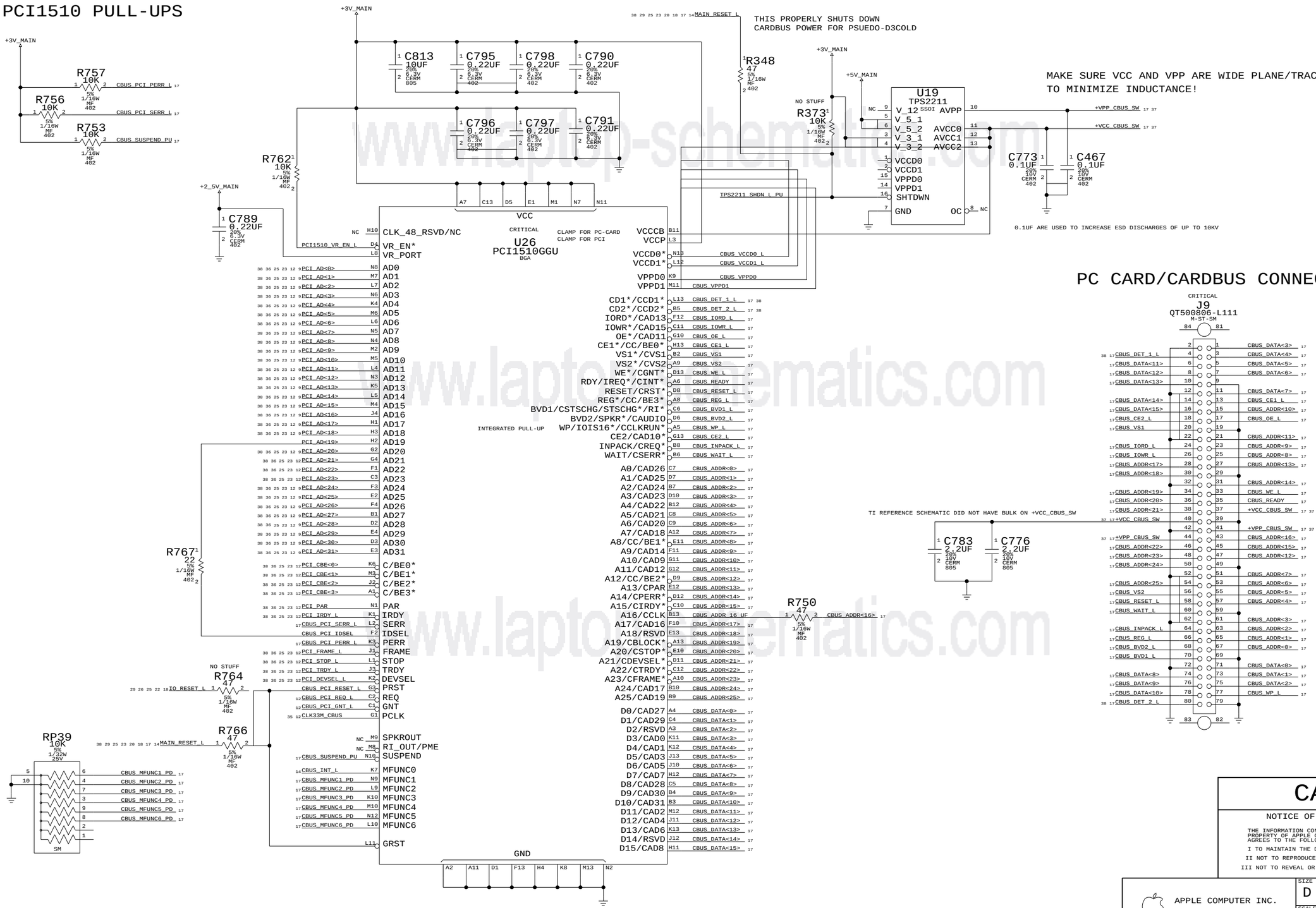
PCI1510 PULL-UPS



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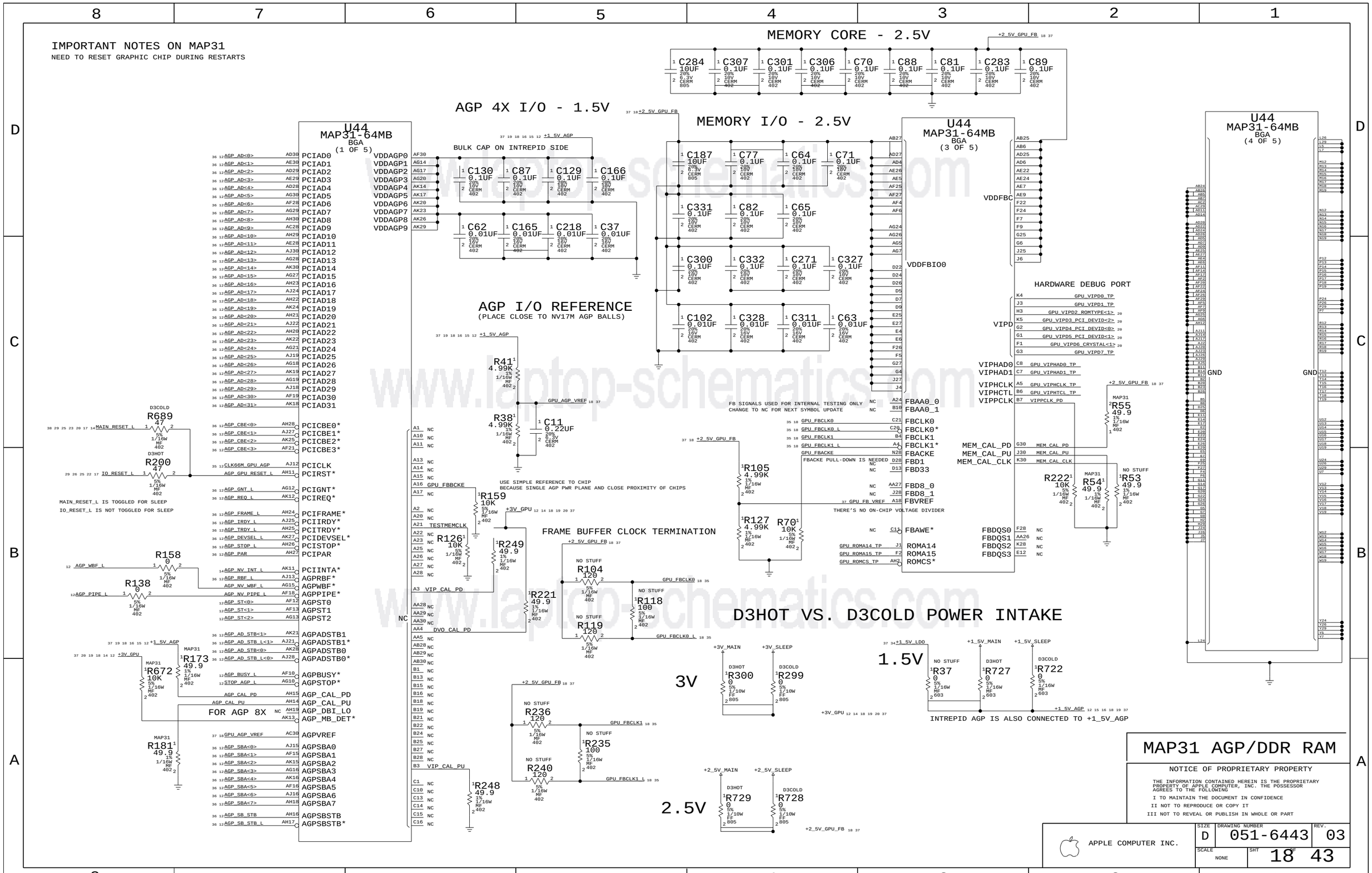
IMPORTANT NOTES ON MAP31
NEED TO RESET GRAPHIC CHIP DURING RESTARTS
MEMORY CORE - 2.5V
AGP 4X I/O - 1.5V
MEMORY I/O - 2.5V
U44
MAP31-64MB
BGA
(1 OF 5)
(3 OF 5)
(4 OF 5)
BULK CAP ON INTREPID SIDE
AGP I/O REFERENCE
(PLACE CLOSE TO NV17M AGP BALLS)
USE SIMPLE REFERENCE TO CHIP
BECAUSE SINGLE AGP PWR PLANE AND CLOSE PROXIMITY OF CHIPS
FRAME BUFFER CLOCK TERMINATION
HARDWARE DEBUG PORT
FB SIGNALS USED FOR INTERNAL TESTING ONLY
CHANGE TO NC FOR NEXT SYMBOL UPDATE
FBACKE PULL-DOWN IS NEEDED
THERE'S NO ON-CHIP VOLTAGE DIVIDER
MAIN_RESET_L IS TOGGLED FOR SLEEP
IO_RESET_L IS NOT TOGGLED FOR SLEEP
FOR AGP 8X
D3HOT VS. D3COLD POWER INTAKE
3V
2.5V
1.5V
INTREPID AGP IS ALSO CONNECTED TO +1_5V_AGP
MAP31 AGP/DDR RAM
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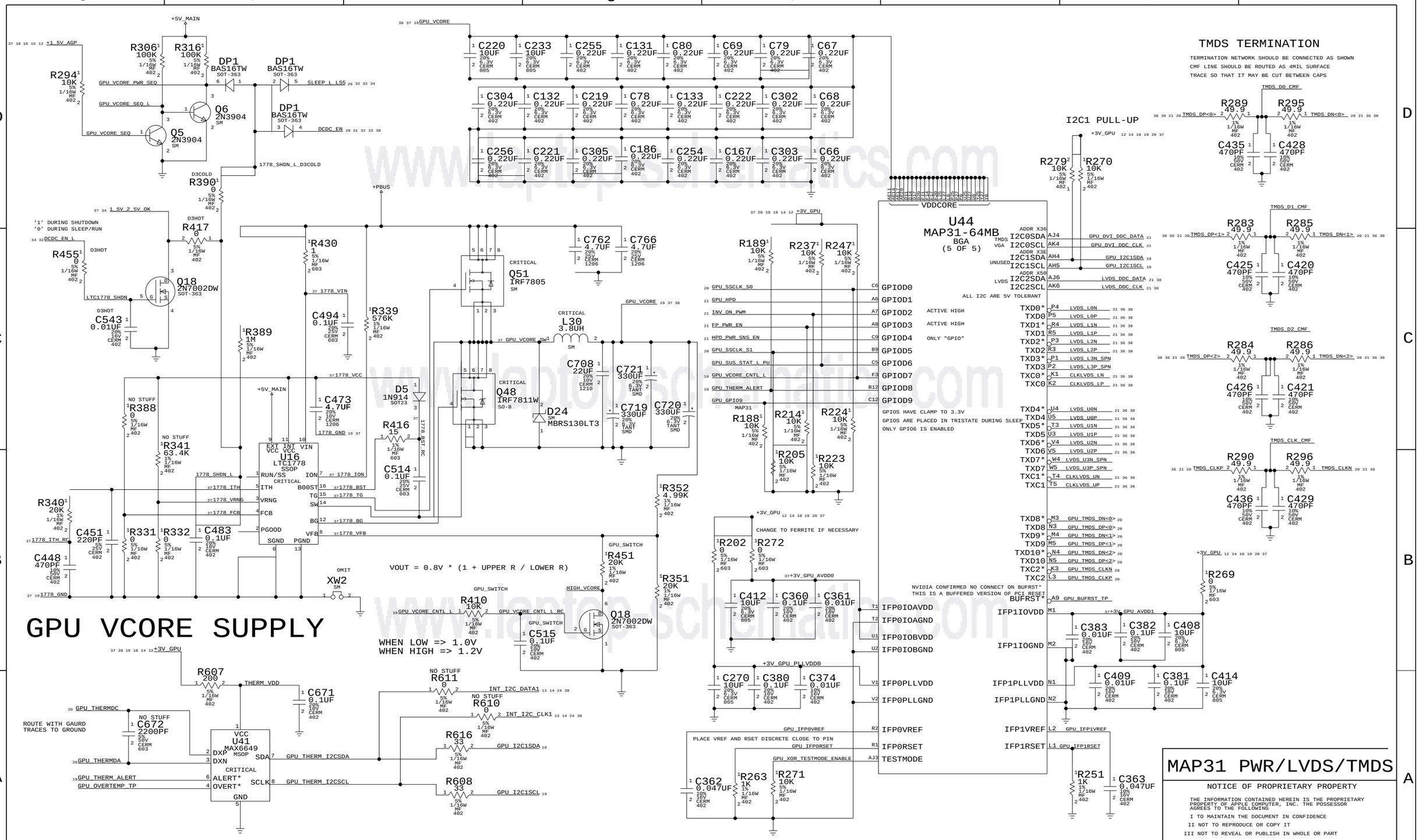
DRAWING NUMBER 051-6443
REV. 03
SCALE NONE
SHT 18 OF 43


TMDS TERMINATION
TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS
I2C1 PULL-UP
U44
MAP31-64MB
BGA
(5 OF 5)
VDDCORE
ALL I2C ARE 5V TOLERANT
GPIOS HAVE CLAMP TO 3.3V
GPIOS ARE PLACED IN TRISTATE DURING SLEEP
ONLY GPIO6 IS ENABLED
NVIDIA CONFIRMED NO CONNECT ON BUFRST*
THIS IS A BUFFERED VERSION OF PCI RESET
GPU VCORE SUPPLY
VOUT = 0.8V * (1 + UPPER R / LOWER R)
WHEN LOW => 1.0V
WHEN HIGH => 1.2V
U16
LTC1778
SSOP
U41
MAX6649
MSOP
CRITICAL
Q51
IRF7805
Q48
IRF7811W
L30
3.8UH
D24
MBRS130LT3
Q18
2N7002DW
SOT-363
XW2
OMIT
PLACE VREF AND RSET DISCRETE CLOSE TO PIN
CHANGE TO FERRITE IF NECESSARY
ROUTE WITH GAURD
TRACES TO GROUND
'1' DURING SHUTDOWN
'0' DURING SLEEP/RUN
MAP31 PWR/LVDS/TMDS
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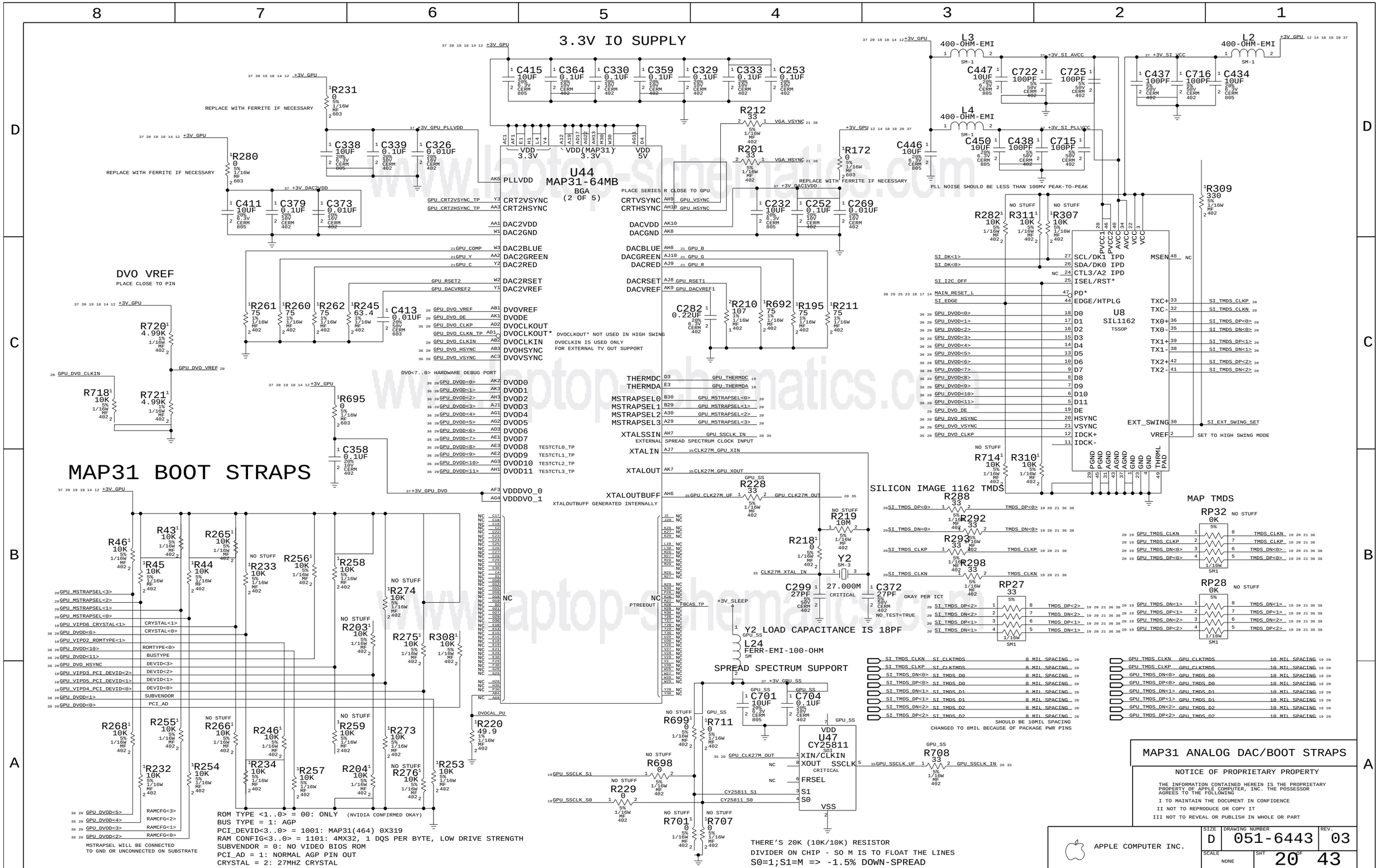
3.3V IO SUPPLY
U44
MAP31-64MB
BGA
(2 OF 5)
DVO VREF
PLACE CLOSE TO PIN
MAP31 BOOT STRAPS
U8
SIL1162
TSSOP
SILICON IMAGE 1162 TMDS
MAP TMDS
U47
CY25811
SPREAD SPECTRUM SUPPORT
MAP31 ANALOG DAC/BOOT STRAPS
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REV. 03
SCALE NONE
SHT 20 OF 43
ROM TYPE <1..0> = 00: ONLY (NVIDIA CONFIRMED OKAY)
BUS TYPE = 1: AGP
PCI_DEVID<3..0> = 1001: MAP31(464) 0X319
RAM CONFIG<3..0> = 1101: 4MX32, 1 DQS PER BYTE, LOW DRIVE STRENGTH
SUBVENDOR = 0: NO VIDEO BIOS ROM
PCI_AD = 1: NORMAL AGP PIN OUT
CRYSTAL = 2: 27MHZ CRYSTAL
MSTRAPSEL WILL BE CONNECTED TO GND OR UNCONNECTED ON SUBSTRATE
THERE'S 20K (10K/10K) RESISTOR
DIVIDER ON CHIP - SO M IS TO FLOAT THE LINES
S0=1;S1=M => -1.5% DOWN-SPREAD
Y2 LOAD CAPACITANCE IS 18PF
PLL NOISE SHOULD BE LESS THAN 100MV PEAK-TO-PEAK
SHOULD BE 10MIL SPACING CHANGED TO 8MIL BECAUSE OF PACKAGE PWR PINS
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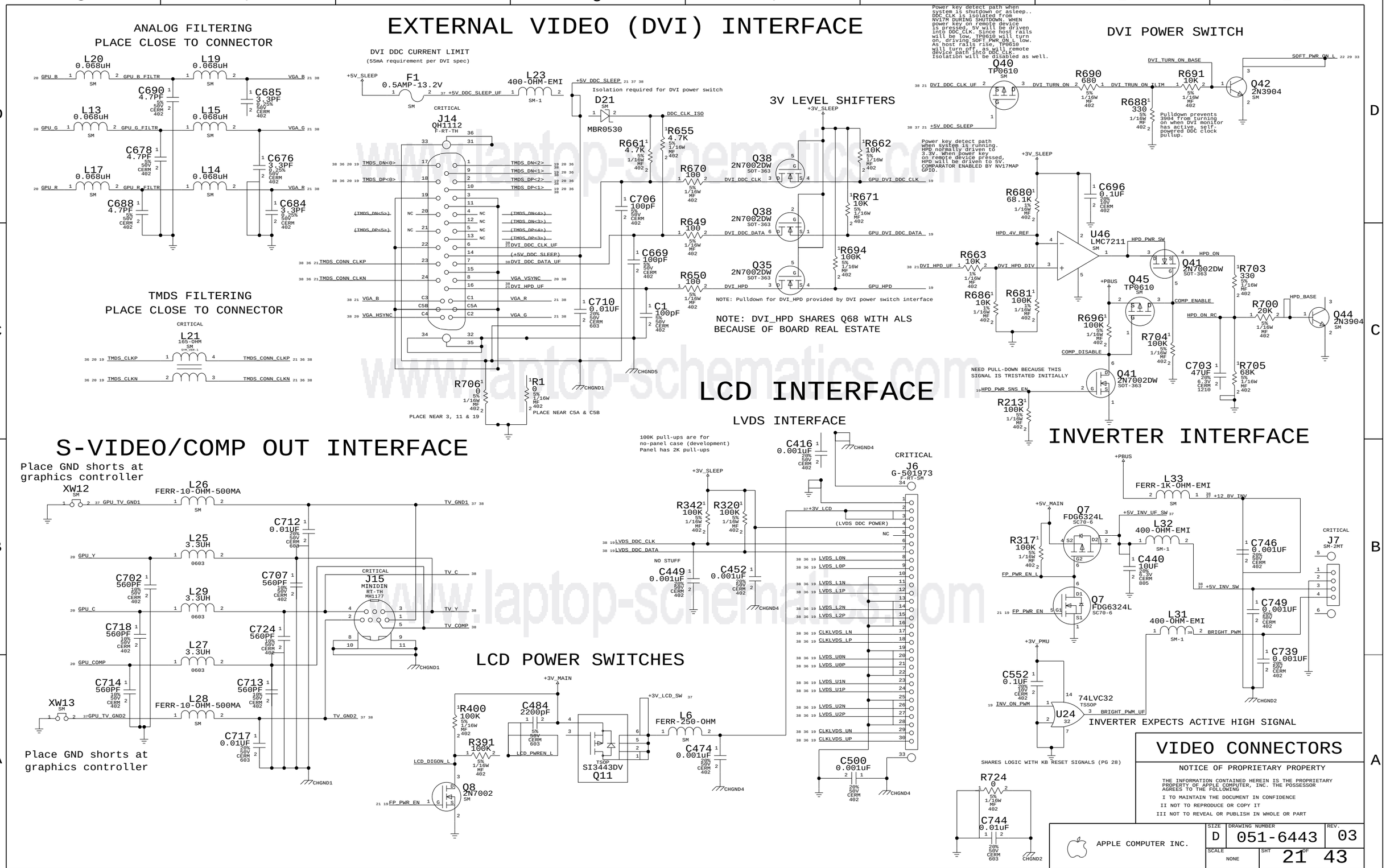
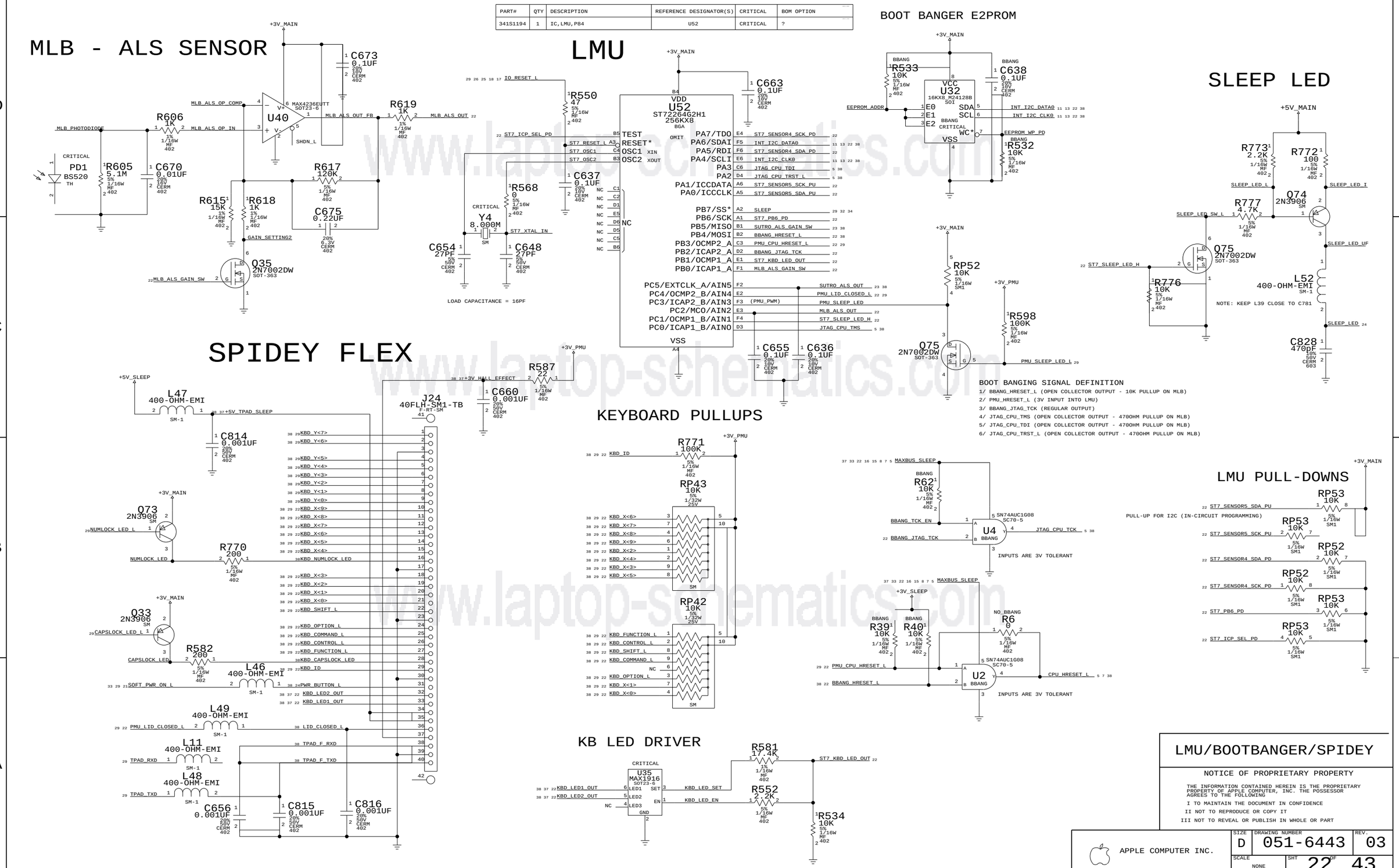
EXTERNAL VIDEO (DVI) INTERFACE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1194	1	IC,LMU,P84	U52	CRITICAL	?



LMU/BOOTBANGER/SPIDEY

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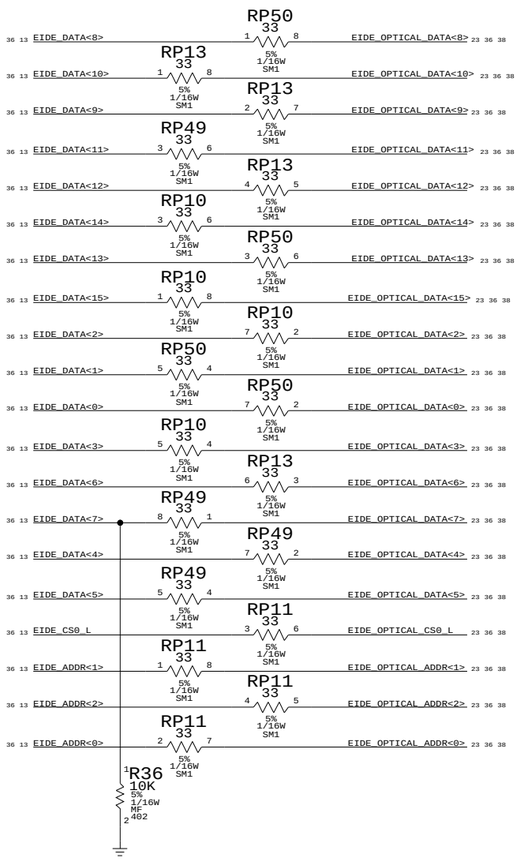
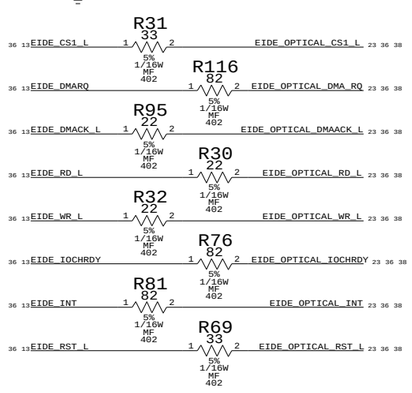
HARD DRIVE INTERFACE (UATA100)

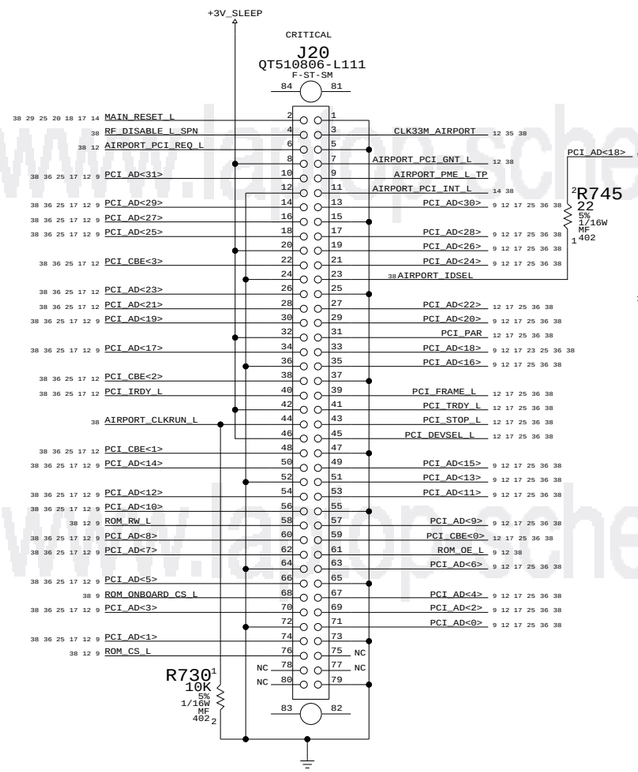
EIDE SERIES TERMINATION

PLACE TERMINATORS NEAR INTREPID

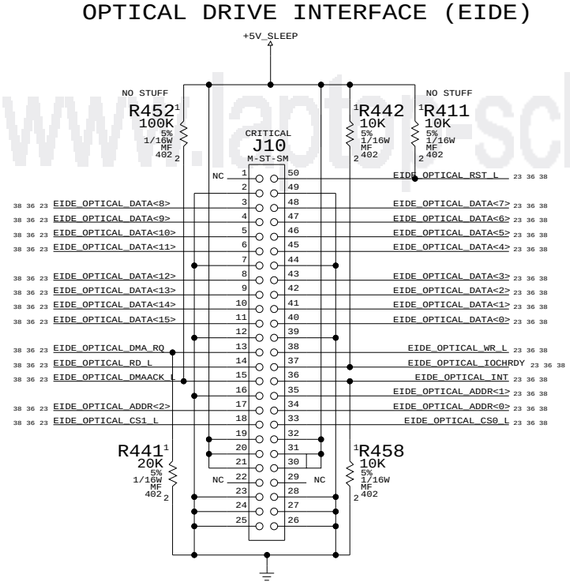




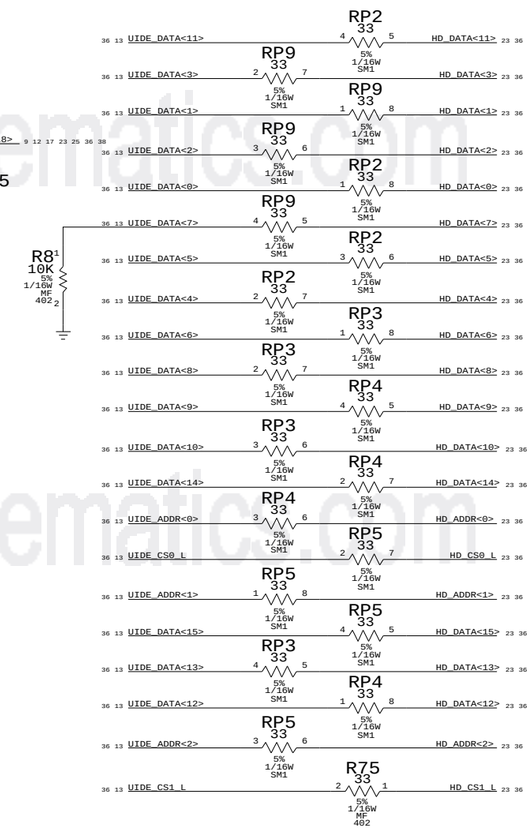
WIRELESS INTERFACE



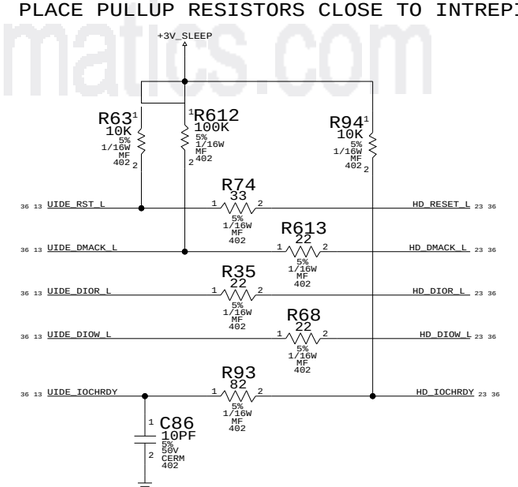
OPTICAL DRIVE INTERFACE (EIDE)



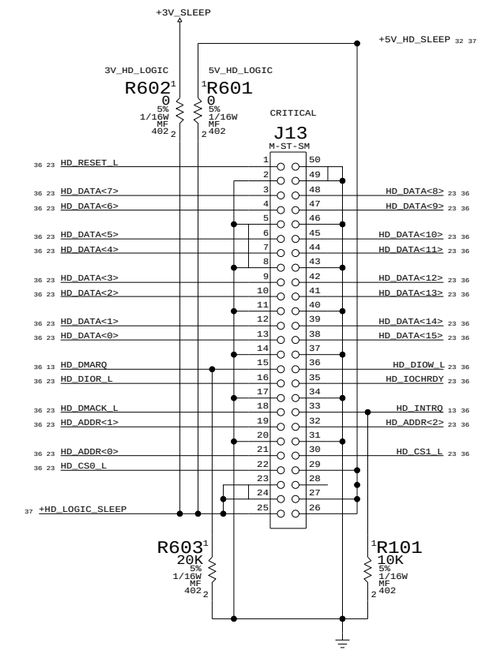
PLACE SERIES R CLOSE TO INTERPID



PLACE PULLUP RESISTORS CLOSE TO INTREPID

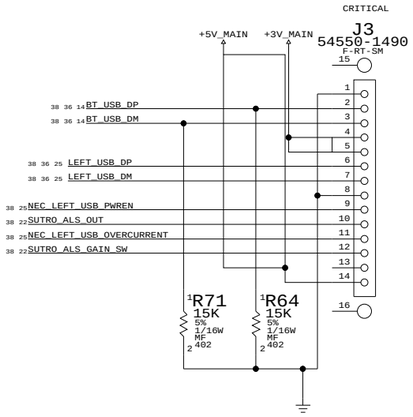


IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V



ANY SEQUENCING REQUIREMENT BETWEEN
+5V_HD_SLEEP AND +3V_SLEEP?

BLUETOOTH/LEFT-SIDE USB



INTERNAL I/O CONNECTORS

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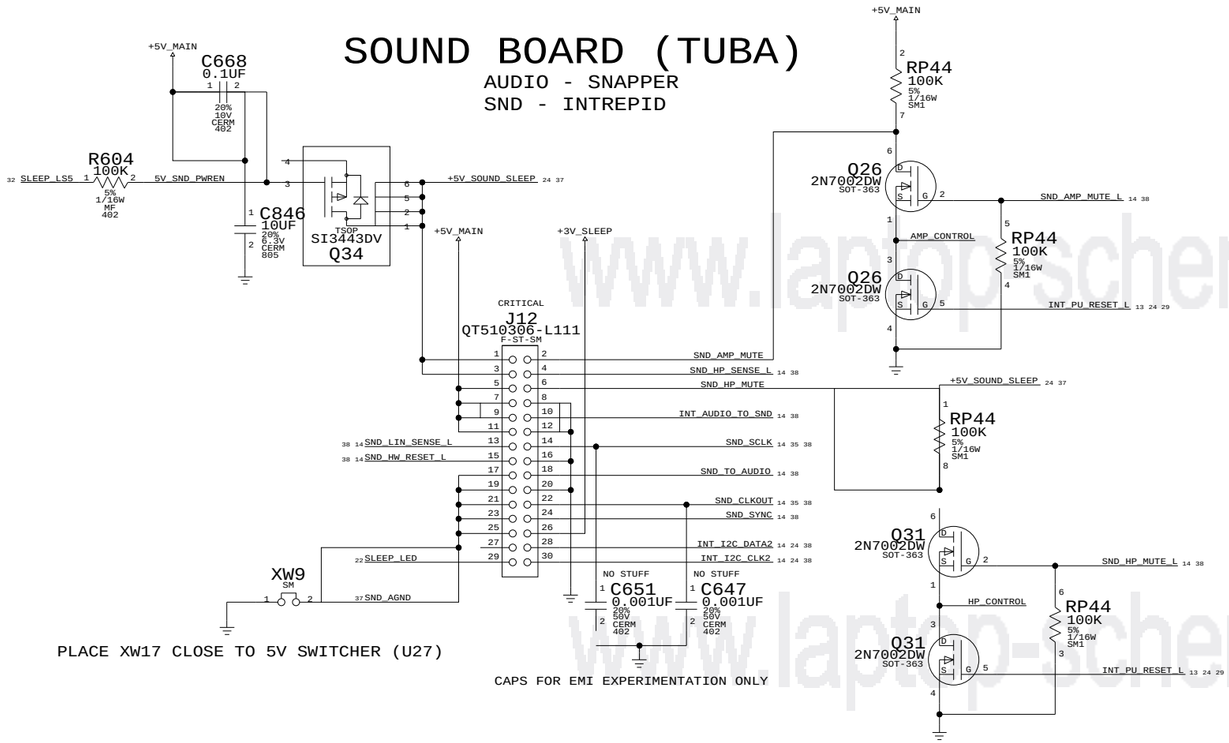
SOUND BOARD (TUBA)

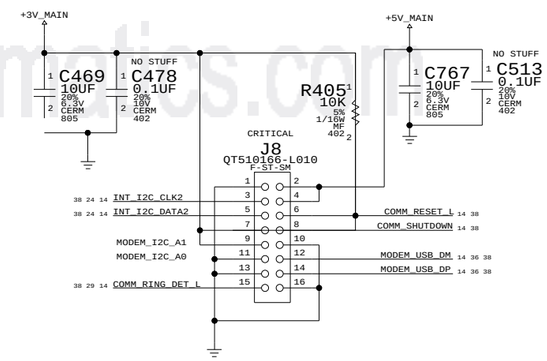
AUDIO - SNAPPER
SND - INTREPID



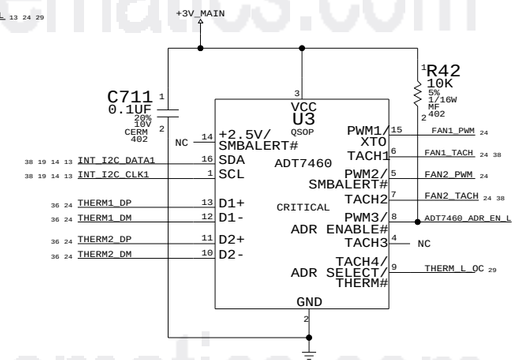
PLACE XW17 CLOSE TO 5V SWITCHER (U27)

CAPS FOR EMI EXPERIMENTATION ONLY

MODEM

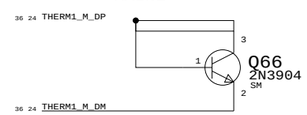


FAN CONTROLLER

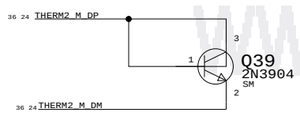


FAN INTERFACE

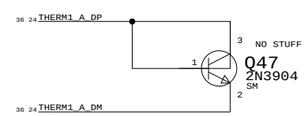
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY
MAIN1



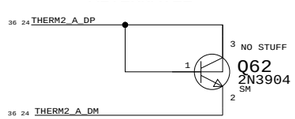
PLACE CLOSE TO CPU
MAIN2



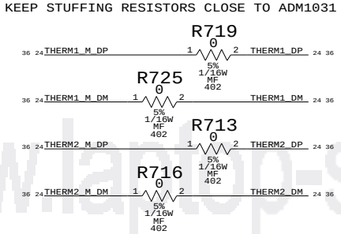
PLACE UNDERNEATH UPPER RAM
ALTERNATE1



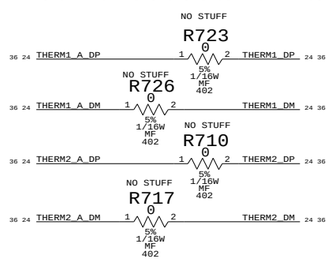
PLACE CLOSE TO BATTERY CHARGER/VCORE
ALTERNATE2



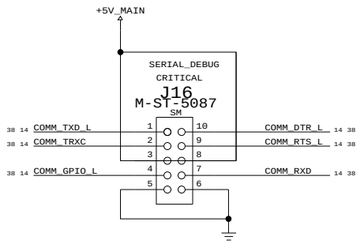
KEEP STUFFING RESISTORS CLOSE TO ADM1031 CONTROLLER



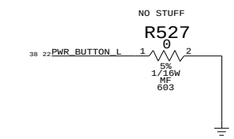
KEEP STUFFING RESISTORS CLOSE TO ADM1031 CONTROLLER



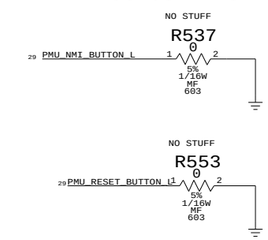
SERIAL DEBUG INTERFACE

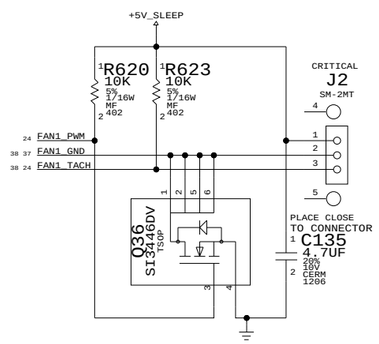


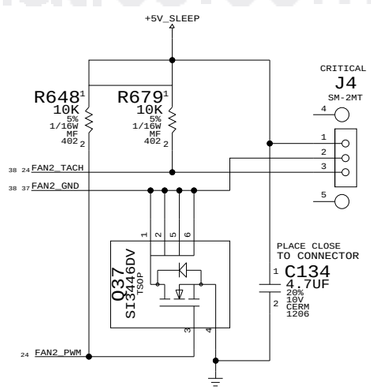
DEBUG POWER BUTTON



DEBUG JUMPERS







FAN/MODEM/SOUND/SLEEP LED/DEBUG

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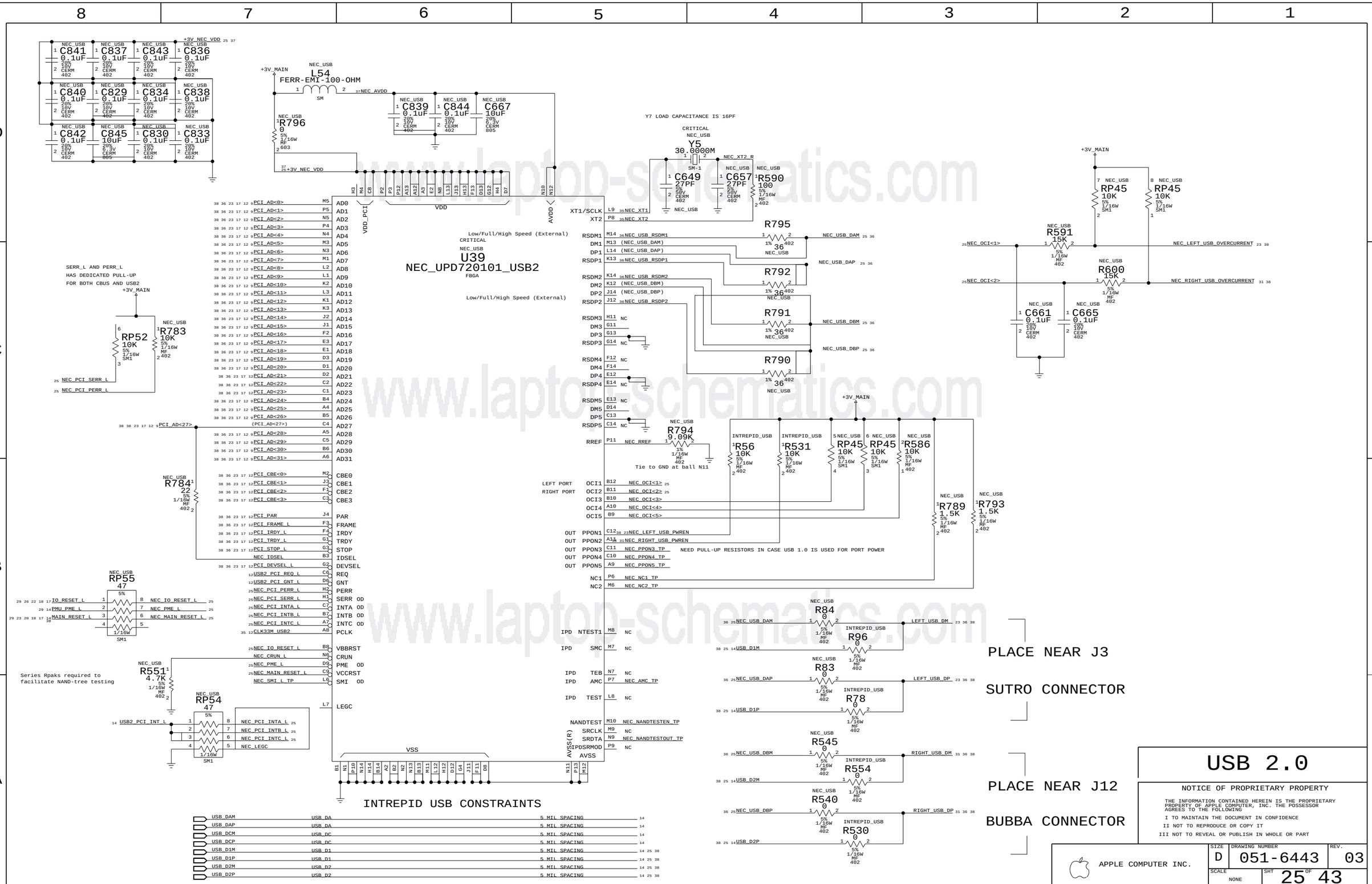
NEC_UPD720101_USB2
U39
FBGA
Y7 LOAD CAPACITANCE IS 16PF
Y5
30.0000M
SERR_L AND PERR_L
HAS DEDICATED PULL-UP
FOR BOTH CBUS AND USB2
Series Rpaks required to
facilitate NAND-tree testing
Low/Full/High Speed (External)
NEED PULL-UP RESISTORS IN CASE USB 1.0 IS USED FOR PORT POWER
Tie to GND at ball N11
INTREPID USB CONSTRAINTS
PLACE NEAR J3
SUTRO CONNECTOR
PLACE NEAR J12
BUBBA CONNECTOR
USB 2.0
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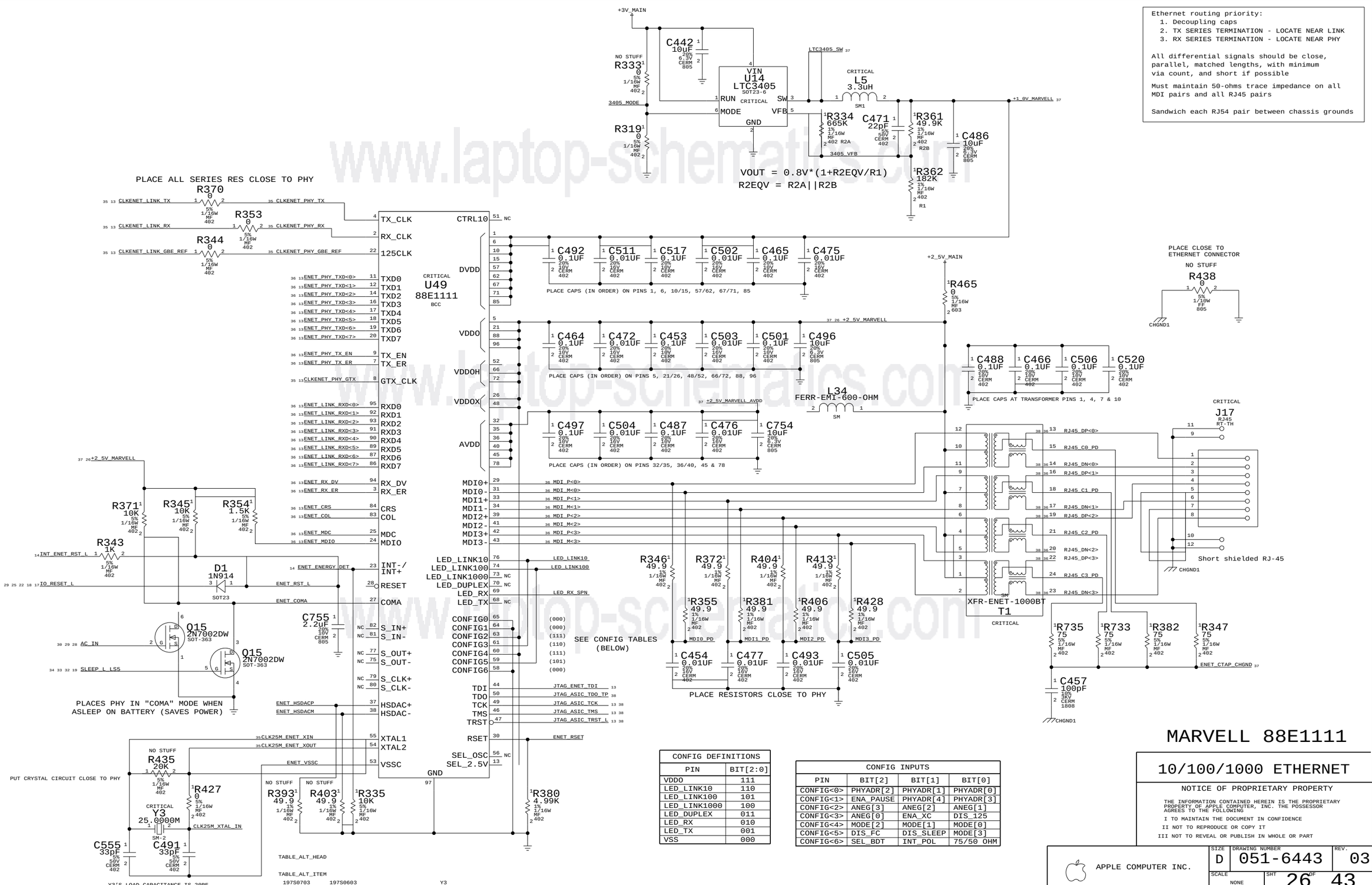
SCALE NONE
SHT 25 OF 43

Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds



CONFIG DEFINITIONS	
PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS			
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

MARVELL 88E1111

10/100/1000 ETHERNET

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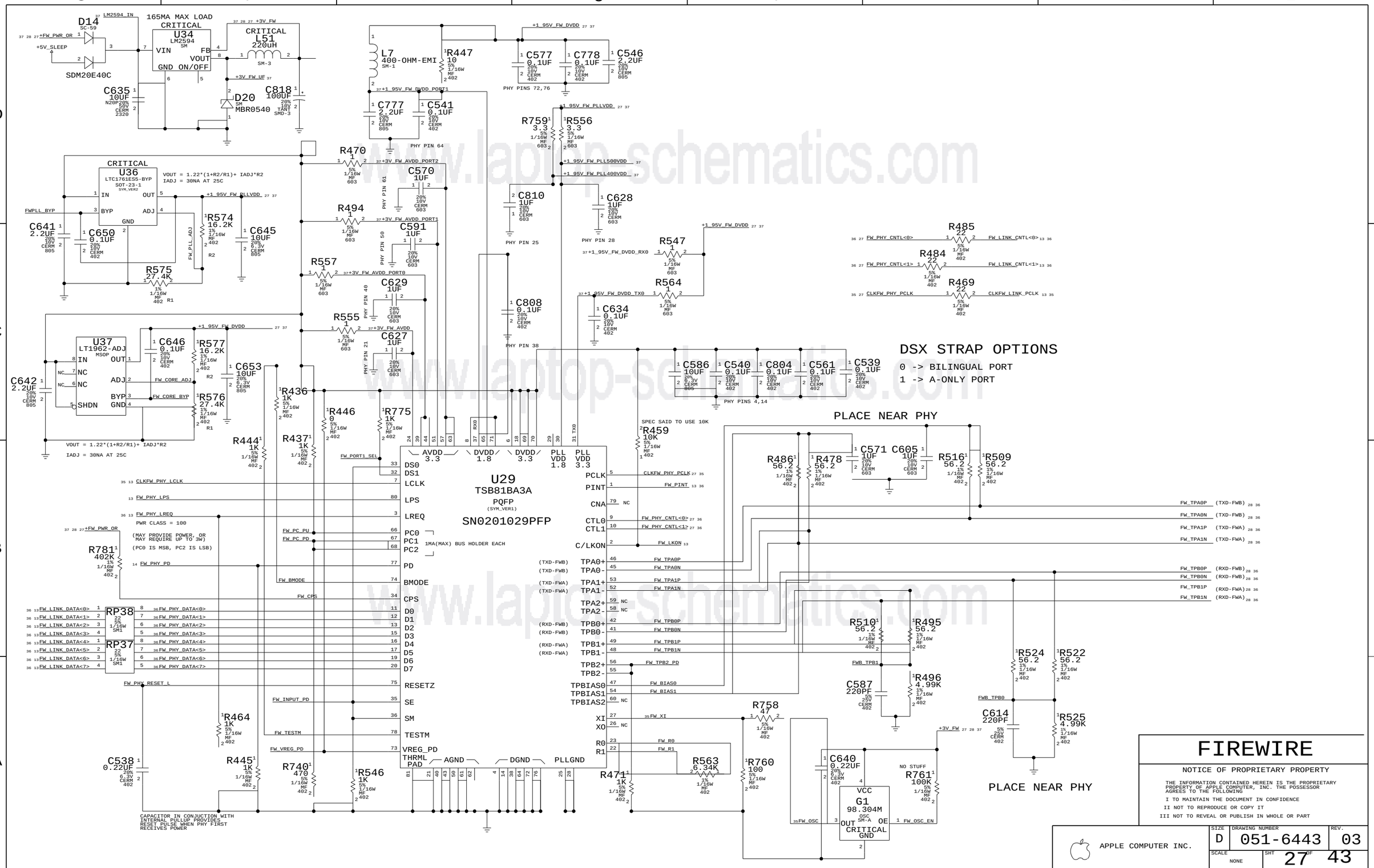

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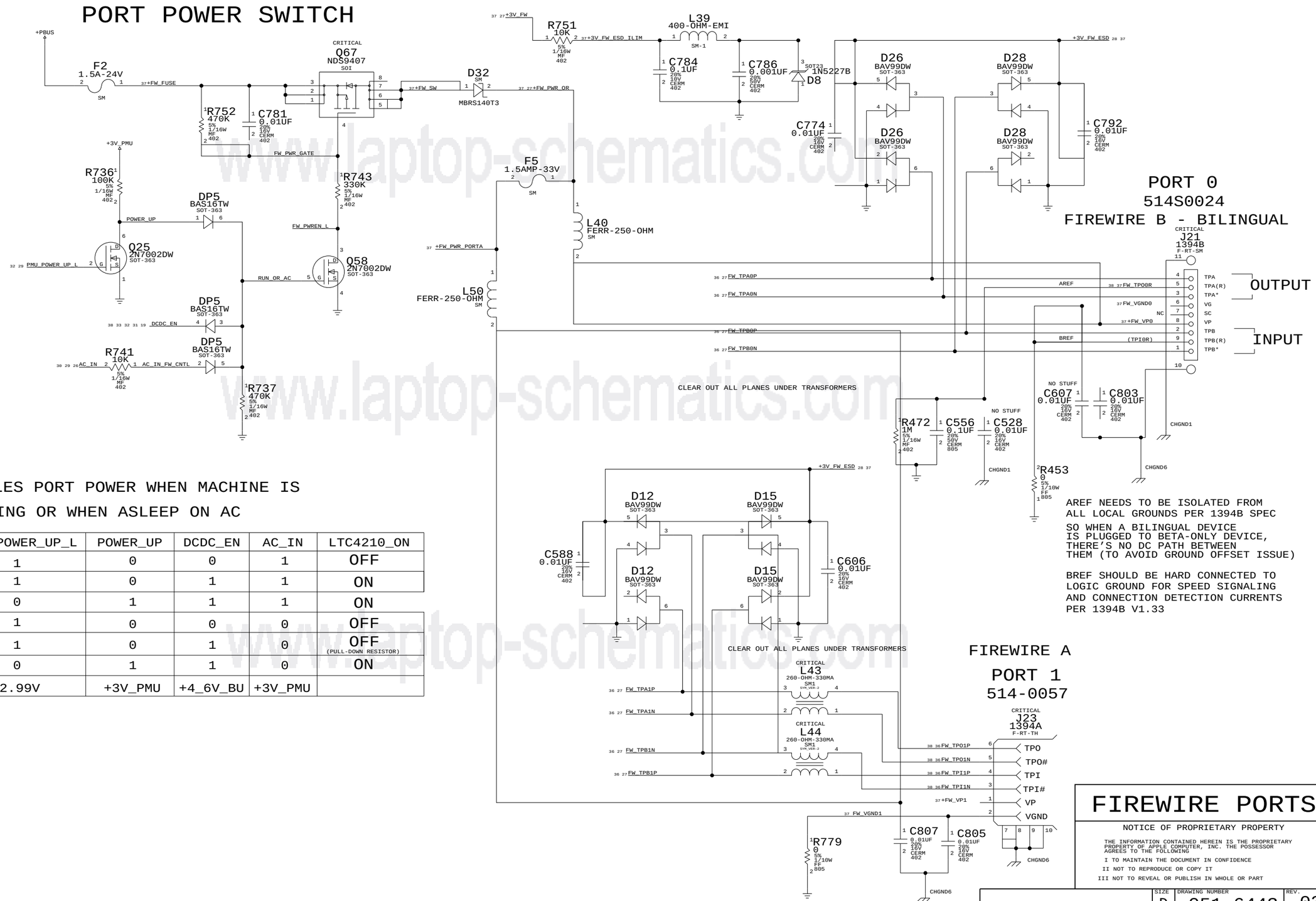
PORT POWER SWITCH



ENABLES PORT POWER WHEN MACHINE IS RUNNING OR WHEN ASLEEP ON AC

STATE	PMU_POWER_UP_L	POWER_UP	DCDC_EN	AC_IN	LTC4210_ON
SHUTDOWN (AC)	1	0	0	1	OFF
SLEEP (AC)	1	0	1	1	ON
RUN (AC)	0	1	1	1	ON
SHUTDOWN (BATT)	1	0	0	0	OFF
SLEEP (BATT)	1	0	1	0	OFF (PULL-DOWN RESISTOR)
RUN (BATT)	0	1	1	0	ON
	2.99V	+3V_PMU	+4_6V_BU	+3V_PMU	

AREF NEEDS TO BE ISOLATED FROM ALL LOCAL GROUNDS PER 1394B SPEC

SO WHEN A BILINGUAL DEVICE IS PLUGGED TO BETA-ONLY DEVICE, THERE'S NO DC PATH BETWEEN THEM (TO AVOID GROUND OFFSET ISSUE)

BREF SHOULD BE HARD CONNECTED TO LOGIC GROUND FOR SPEED SIGNALING AND CONNECTION DETECTION CURRENTS PER 1394B V1.33

FIREWIRE PORTS

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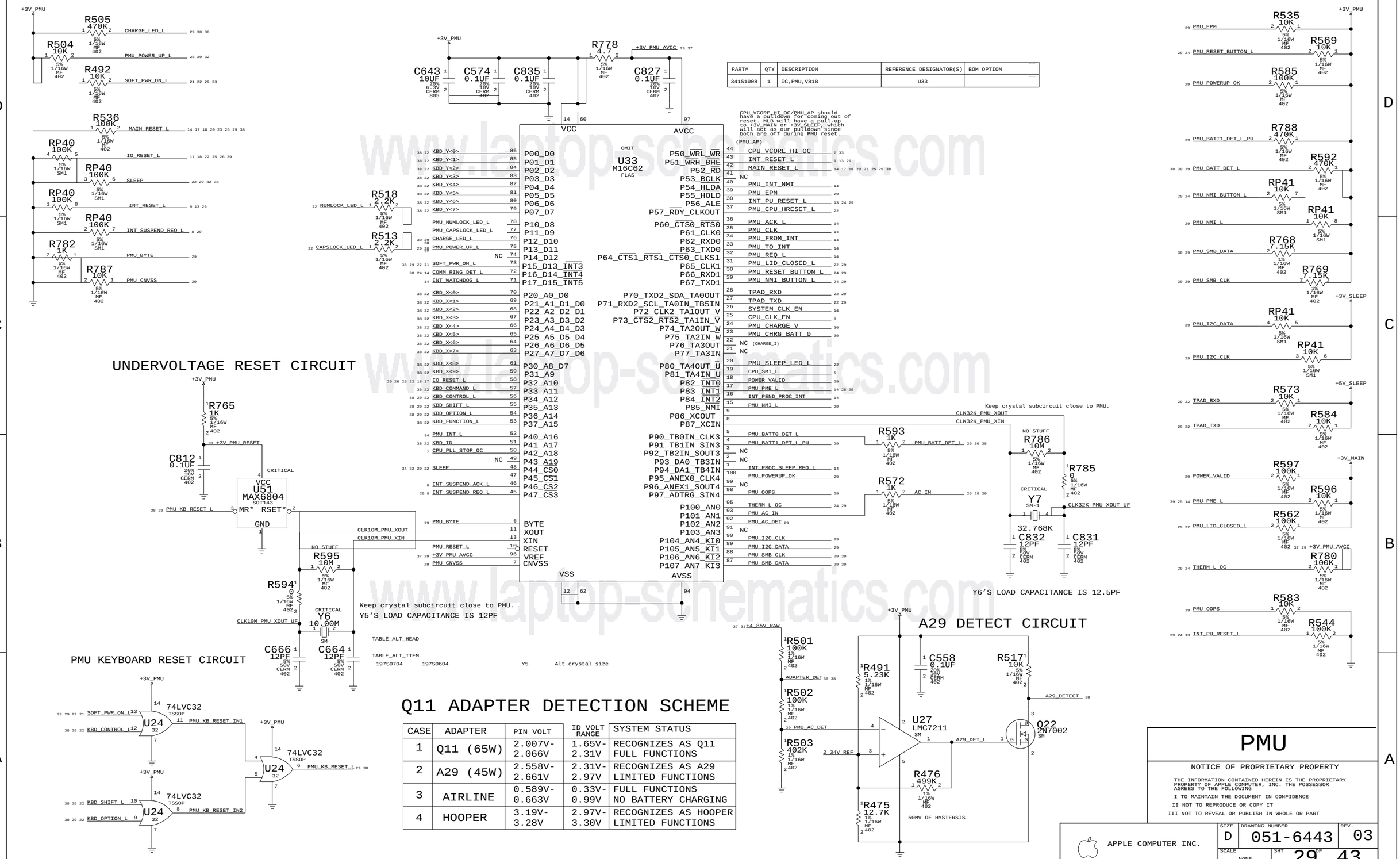

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1008	1	IC,PMU,V81B	U33	

Q11 ADAPTER DETECTION SCHEME

CASE	ADAPTER	PIN VOLT	ID VOLT RANGE	SYSTEM STATUS
1	Q11 (65W)	2.007V- 2.066V	1.65V- 2.31V	RECOGNIZES AS Q11 FULL FUNCTIONS
2	A29 (45W)	2.558V- 2.661V	2.31V- 2.97V	RECOGNIZES AS A29 LIMITED FUNCTIONS
3	AIRLINE	0.589V- 0.663V	0.33V- 0.99V	FULL FUNCTIONS NO BATTERY CHARGING
4	HOOPER	3.19V- 3.28V	2.97V- 3.30V	RECOGNIZES AS HOOPER LIMITED FUNCTIONS

PMU

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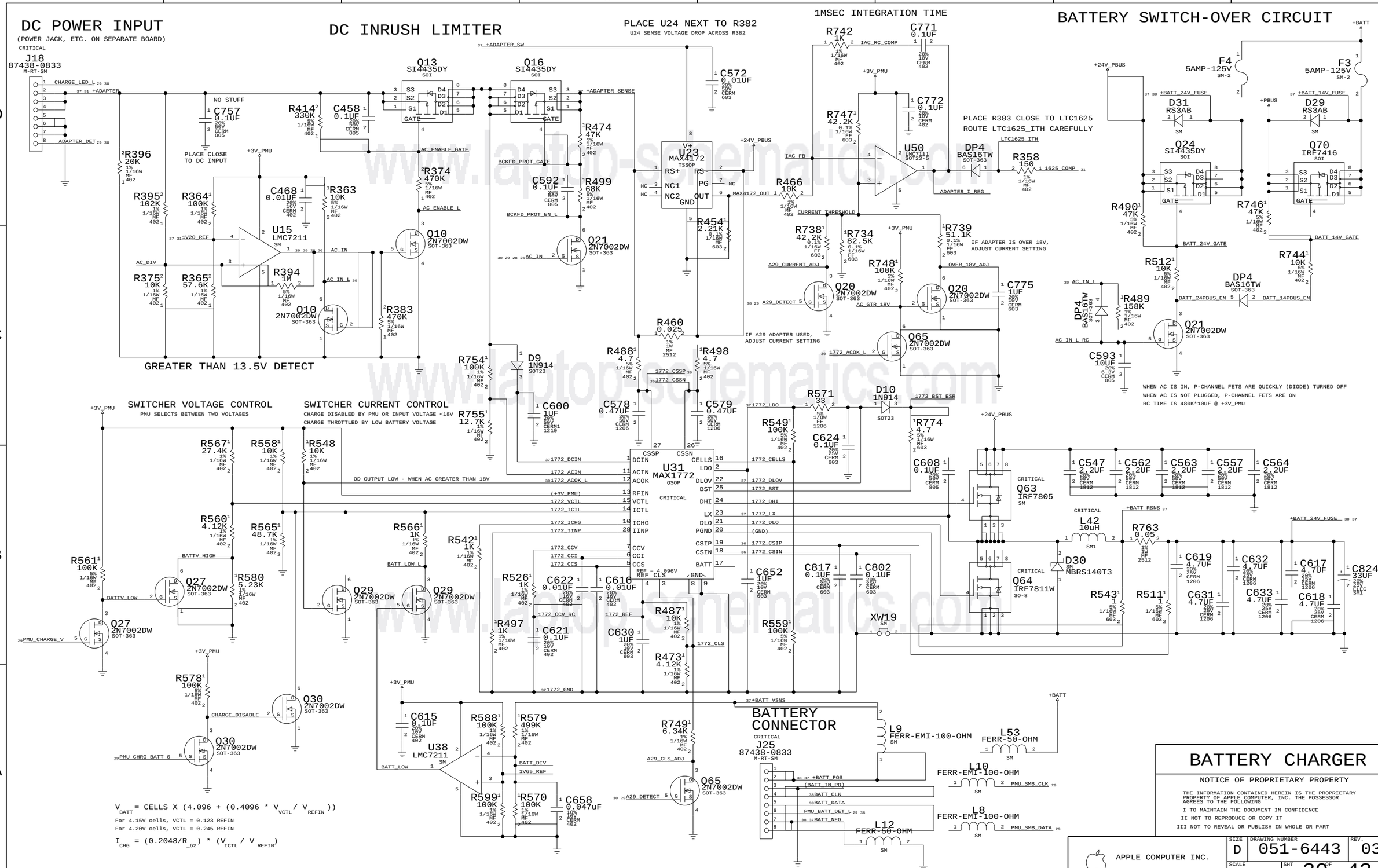
DC POWER INPUT
(POWER JACK, ETC. ON SEPARATE BOARD)
CRITICAL
J18
87438-0833
M-RT-SM
CHARGE_LED_L
+ADAPTER
ADAPTER_DET
NO STUFF
C757
0.1UF
PLACE CLOSE TO DC INPUT
R396
20K
R395
102K
R364
100K
R375
10K
R365
57.6K
C468
0.01UF
R363
10K
U15
LMC7211
R394
1M
Q10
2N7002DW
SOT-363
R383
470K
GREATER THAN 13.5V DETECT
DC INRUSH LIMITER
Q13
SI4435DY
SOI
Q16
SI4435DY
SOI
R414
330K
C458
0.1UF
R374
470K
R474
47K
R499
68K
Q21
2N7002DW
SOT-363
+ADAPTER_SW
+ADAPTER_SENSE
AC_ENABLE_GATE
AC_ENABLE_L
BCKFD_PROT_GATE
BCKFD_PROT_EN_L
AC_IN
AC_DIV
1V20_REF
AC_IN_L
PLACE U24 NEXT TO R382
U24 SENSE VOLTAGE DROP ACROSS R382
C572
0.01UF
U23
MAX4172
TSSOP
RS+
RS-
NC1
NC2
GND
PG
OUT
R454
2.21K
+24V_PBUS
MAX4172_OUT
1MSEC INTEGRATION TIME
R742
1K
C771
0.1UF
IAC_RC_COMP
+3V_PMU
C772
0.1UF
R747
42.2K
U50
LMC7111
SOT23-5
IAC_FB
R466
10K
CURRENT THRESHOLD
PLACE R383 CLOSE TO LTC1625
ROUTE LTC1625_ITH CAREFULLY
DP4
BAS16TW
SOT-363
LTC1625_ITH
R358
150
1625_COMP
ADAPTER_I_REG
R738
42.2K
R734
82.5K
R739
51.1K
IF ADAPTER IS OVER 18V,
ADJUST CURRENT SETTING
A29_CURRENT_ADJ
R748
100K
OVER_18V_ADJ
Q20
2N7002DW
SOT-363
C775
1UF
A29_DETECT
AC_GTR_18V
Q65
2N7002DW
SOT-363
1772_ACOK_L
R460
0.025
IF A29 ADAPTER USED,
ADJUST CURRENT SETTING
R488
4.7
R498
4.7
1772_CSSP
1772_CSSN
R754
100K
D9
1N914
SOT23
C600
1UF
R755
12.7K
C578
0.47UF
C579
0.47UF
R571
33
D10
1N914
SOT23
1772_BST_ESR
R549
100K
C624
0.1UF
R774
4.7
1772_LDO
1772_DCIN
1772_ACIN
1772_ACOK_L
(+3V_PMU)
1772_VCTL
1772_ICTL
1772_ICHG
1772_IINP
1772_CCV
1772_CCI
1772_CCS
1772_CCV_RC
1772_REF
1772_GND
1772_CELLS
1772_DLOV
1772_BST
1772_DHI
1772_LX
1772_DLO
(GND)
1772_CSIP
1772_CSIN
1772_CLS
U31
MAX1772
QSOP
CRITICAL
CSSP
CSSN
DCIN
ACIN
ACOK
RFIN
VCTL
ICTL
ICHG
IINP
CCV
CCI
CCS
REF = 4.096V
REF_CLS
CELLS
LDO
DLOV
BST
DHI
LX
DLO
PGND
CSIP
CSIN
BATT
GND
SWITCHER VOLTAGE CONTROL
PMU SELECTS BETWEEN TWO VOLTAGES
SWITCHER CURRENT CONTROL
CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V
CHARGE THROTTLED BY LOW BATTERY VOLTAGE
OD OUTPUT LOW - WHEN AC GREATER THAN 18V
R567
27.4K
R558
10K
R548
10K
R560
4.12K
R565
48.7K
R561
100K
R580
5.23K
BATTV_HIGH
BATTV_LOW
Q27
2N7002DW
SOT-363
PMU_CHARGE_V
R566
1K
BATT_LOW_L
Q29
2N7002DW
SOT-363
R542
1K
R526
1K
C622
0.01UF
C616
0.01UF
R497
1K
C621
0.1UF
C630
1UF
R487
10K
R473
4.12K
C652
1UF
C817
0.1UF
C802
0.1UF
R559
100K
XW19
C608
0.1UF
Q63
IRF7805
SM
Q64
IRF7811W
SO-8
CRITICAL
C547
2.2UF
C562
2.2UF
C563
2.2UF
C557
2.2UF
C564
2.2UF
L42
10uH
SM1
D30
SM
MBRS140T3
R763
0.05
+BATT_RSNS
R543
1
R511
1
C619
4.7UF
C631
4.7UF
C632
4.7UF
C633
4.7UF
C617
4.7UF
C618
4.7UF
C824
33UF
ELEC
SM1
+BATT_24V_FUSE
R578
100K
Q30
2N7002DW
SOT-363
CHARGE_DISABLE
PMU_CHRG_BATT_0
C615
0.1UF
U38
LMC7211
SM
BATT_LOW
R588
100K
R579
499K
BATT_DIV
1V65_REF
R599
100K
R570
100K
C658
0.047uF
R749
6.34K
A29_CLS_ADJ
A29_DETECT
BATTERY CONNECTOR
CRITICAL
J25
87438-0833
M-RT-SM
+BATT_VSNS
+BATT_POS
(BATT_IN_PD)
BATT_CLK
BATT_DATA
PMU_BATT_DET_L
BATT_NEG
L9
FERR-EMI-100-OHM
SM
L53
FERR-50-OHM
L10
FERR-EMI-100-OHM
PMU_SMB_CLK
L8
FERR-EMI-100-OHM
PMU_SMB_DATA
L12
FERR-50-OHM
+BATT
BATTERY SWITCH-OVER CIRCUIT
+24V_PBUS
F4
5AMP-125V
SM-2
F3
5AMP-125V
SM-2
+BATT_24V_FUSE
+BATT_14V_FUSE
D31
RS3AB
SM
D29
RS3AB
SM
+PBUS
Q24
SI4435DY
SOI
Q70
IRF7416
SOI
R490
47K
R746
47K
BATT_24V_GATE
BATT_14V_GATE
R512
10K
R744
10K
DP4
BAS16TW
SOT-363
BATT_24PBUS_EN
BATT_14PBUS_EN
AC_IN_L
R489
158K
AC_IN_L_RC
Q21
2N7002DW
SOT-363
C593
10UF
WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF
WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON
RC TIME IS 480K*10UF @ +3V_PMU
$V_{BATT} = CELLS \times (4.096 + (0.4096 * V_{VCTL} / V_{REFIN}))$
For 4.15V cells, VCTL = 0.123 REFIN
For 4.20V cells, VCTL = 0.245 REFIN
$I_{CHG} = (0.2048/R_{62}) * (V_{ICTL} / V_{REFIN})$
BATTERY CHARGER
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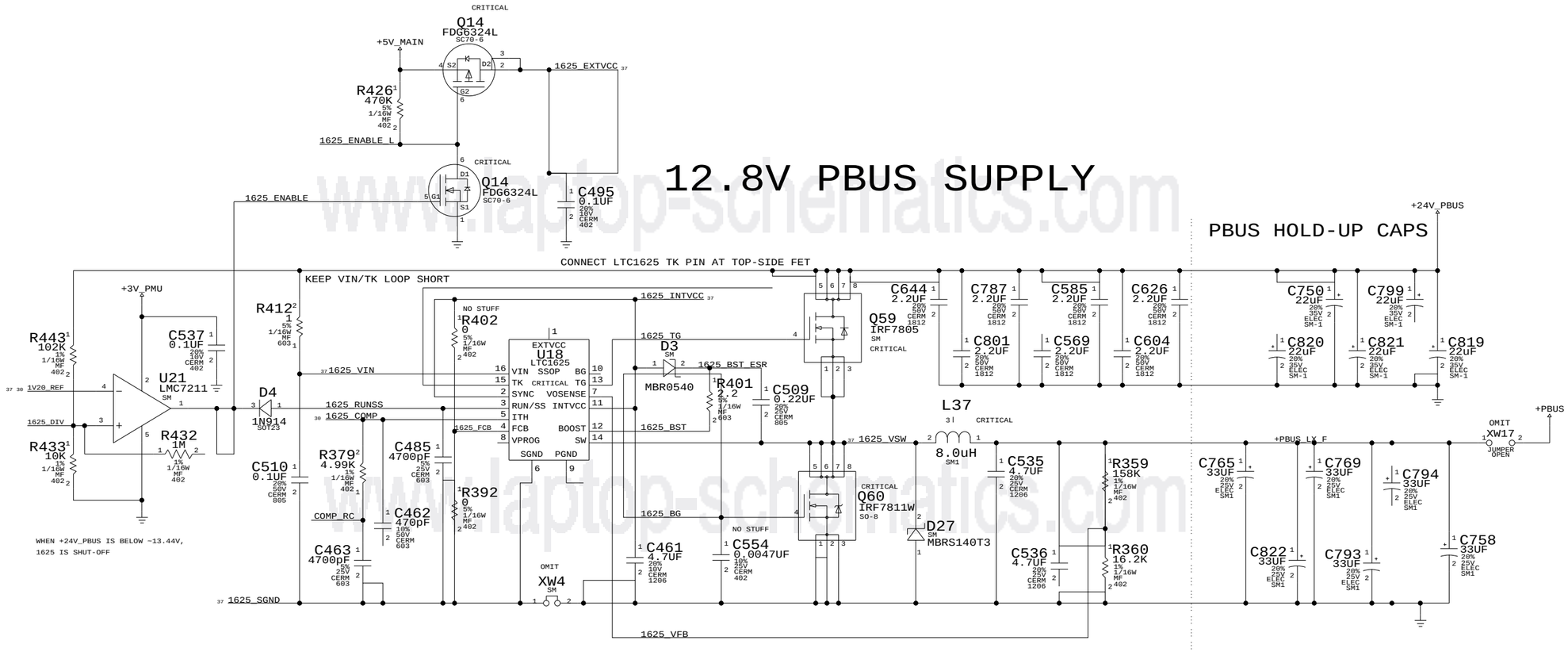
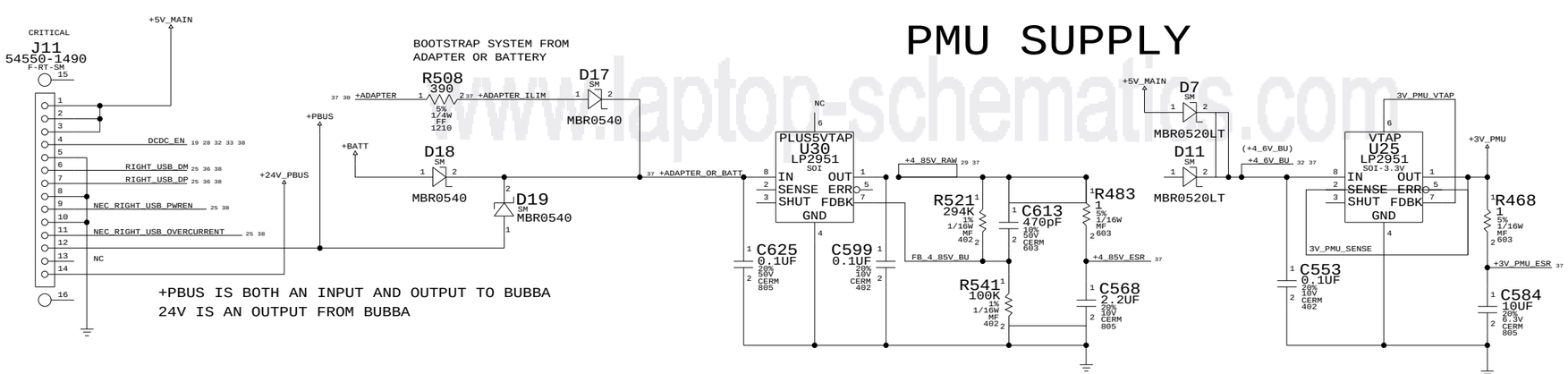
SIZE D
DRAWING NUMBER 051-6443
REV. 03
SCALE NONE
SHT 30 OF 43

12.8V PBUS SUPPLY



BACKUP BATTERY / USB CONNECTOR

PMU SUPPLY



+PBUS IS BOTH AN INPUT AND OUTPUT TO BUBBA
24V IS AN OUTPUT FROM BUBBA

12.8V REGULATOR

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SCALE NONE	SHT 31 OF 43	

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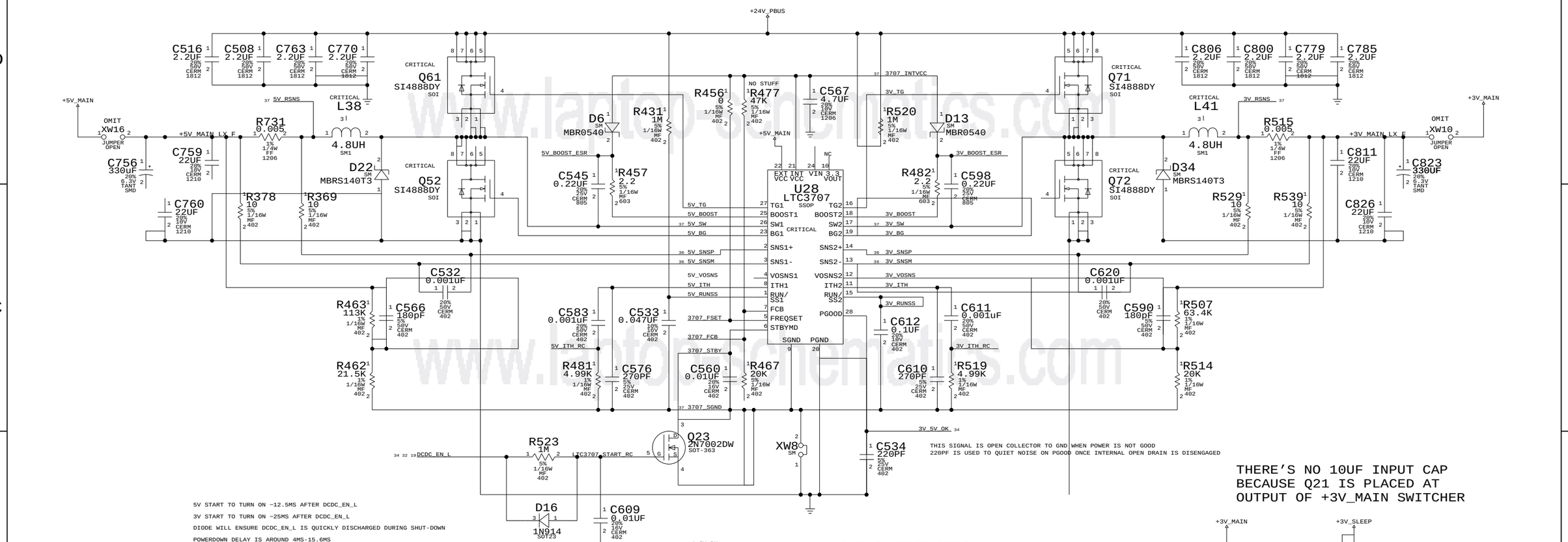
3.3V/5V MAIN SUPPLY



DCDC_EN TRUTH TABLE

PMU_POWER_UP_L	SLEEP	DCDC_EN	DCDC_EN_L	State
0	0	1	0	Run
1 (2.99V)	1	1	0	Sleep
1	0	0	1	Shutdown
+3V_PMU	+3V_PMU	+4_6V_BU	+3V_PMU	VOLTAGE

SLEEP LEVEL SHIFTER (3V -> 5V)

+3V_SLEEP LOADS

1) CPU PLL Config Control
2) INTREPID - IIC AND PCI PULL-UPS
3) MAP31 - 3V RAIL (IF USING D3COLD)
4) GRAPHIC CHIP SPREAD SPECTRUM CHIP
5) LVDS DDC PULL-UPS
6) DVI LEVEL SHIFTERS & PULL-UPS & HPD
7) SOUND BOARD
8) BOOT BANGER
9) HARD DRIVE (IF USING 3V LOGIC)
10) WIRELESS (IF POWERING OFF IN SLEEP)
11) PMU - IIC Pull-ups
12) PCI PULL-UPS

+5V_SLEEP LOADS

1) OPTICAL DRIVE
2) DVI
3) TRACKPAD
4) FANS
5) FIREWIRE PHY

3.3V/5V REGULATOR

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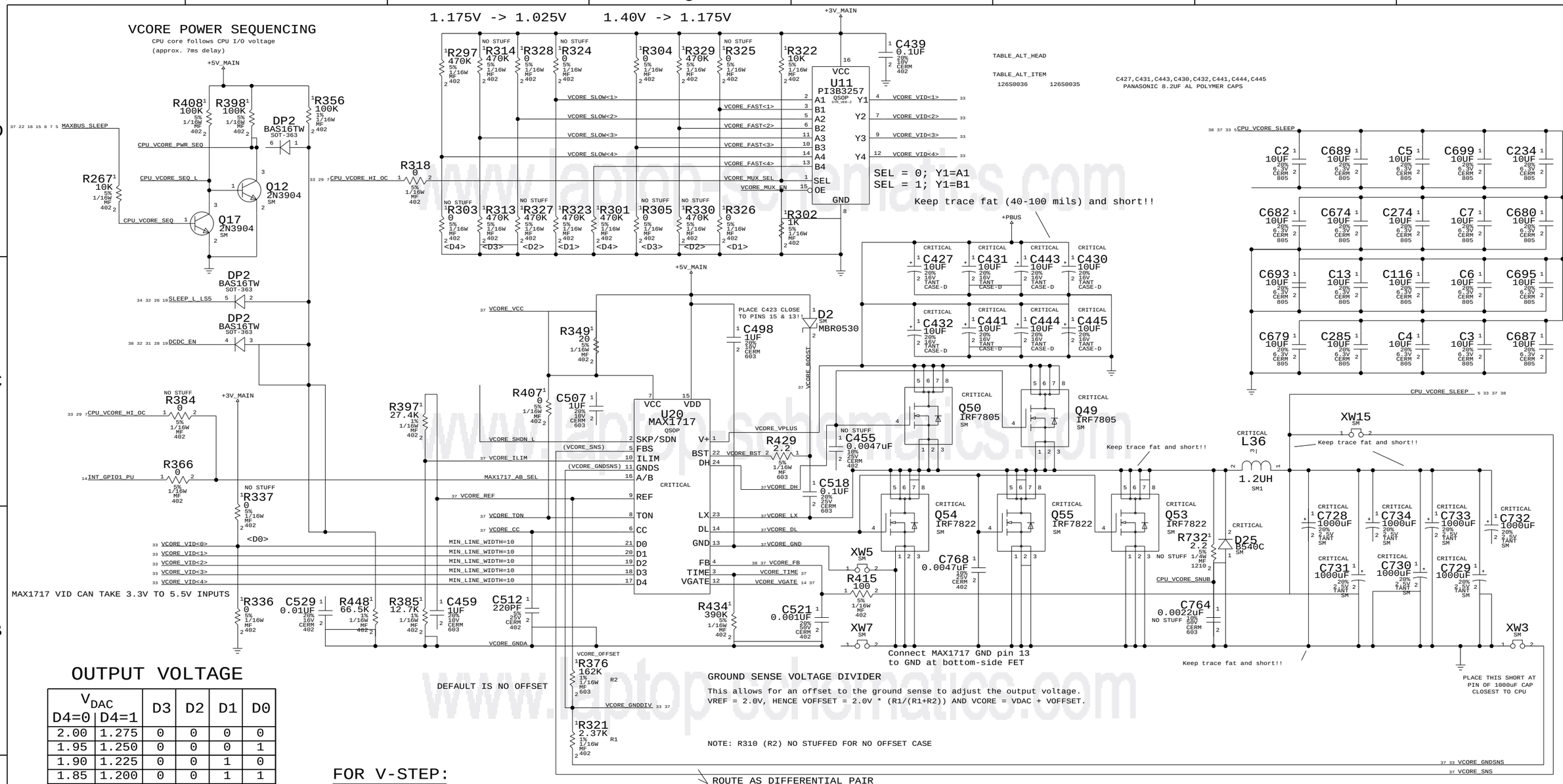

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all pull-downs are <=1K, $V_A = V_B$.

VCORE SUPPLY

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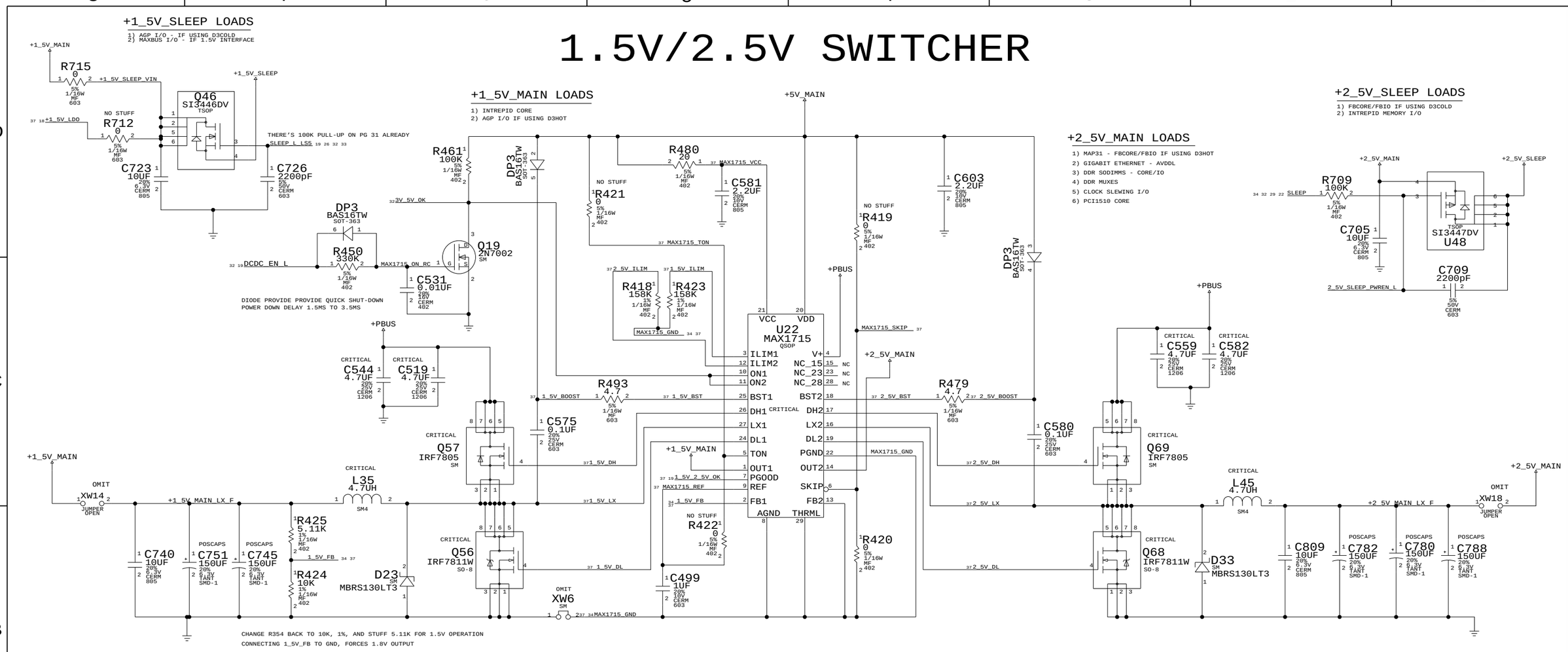
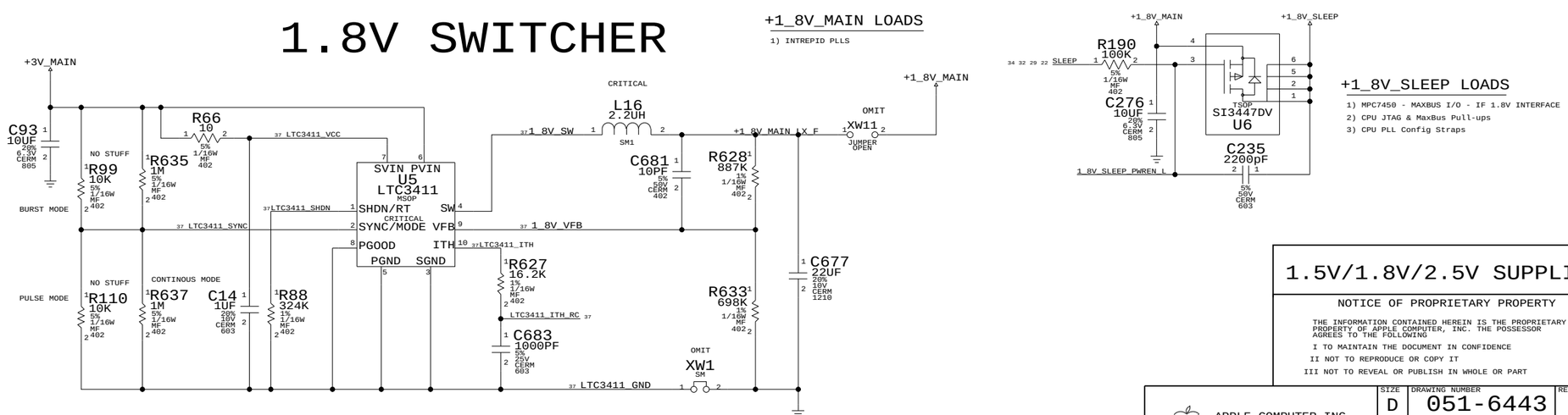
1.5V/2.5V SWITCHER



1.8V SWITCHER



1.5V/1.8V/2.5V SUPPLIES

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SCALE NONE	SHT 34 OF 43	

DIGITAL SIGNALS

GROUP	SIG_NAME	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
MAXBUS	CPU_AACK_L	5		250.0000	10_MIL_SPACING			5 8
	CPU_ADDR<0..31>	5		250			83_MHZ	5 8
	CPU_ARTRY_L	5		250.0000	10_MIL_SPACING			5 8
	CPU_BG_L	5		250.0000	10_MIL_SPACING			5 8
	CPU_BR_L	5		250.0000	10_MIL_SPACING			5 8
	CPU_CI_L	5		250.0000				5 8
	CPU_DATA<0..31>	5		250			83_MHZ	6 8
	CPU_DATA<32..63>	5		250			83_MHZ	6 8
	CPU_DBG_L	5		250.0000	10_MIL_SPACING			5 8
	CPU_DTI<0..2>	5		250				5 8
	CPU_DRDY_L_UF			250.0000	10_MIL_SPACING			
	CPU_DRDY_L	5		250.0000	10_MIL_SPACING			5 8
	CPU_GBL_L	5		250.0000				5 8
	CPU_HIT_L	5		250.0000	10_MIL_SPACING			5 8
	CPU_QACK_L	5		250.0000	10_MIL_SPACING			5 8
	CPU_QREQ_L	5		250.0000	10_MIL_SPACING			5 8
	CPU_TA_L	5		250.0000	10_MIL_SPACING			5 8
	CPU_TBST_L	5		250.0000	10_MIL_SPACING			5 8
	CPU_TEA_L	5		250.0000				5 8
	CPU_TS_L	5		250.0000	10_MIL_SPACING			5 8
	CPU_TSIZ<0..2>	5		250				5 8
	CPU_TT<0..4>	5		250				5 8
	CPU_WT_L	5		250.0000				5 8
GROUP 0	MEM_DATA<7..0>	4		200			167_MHZ	9 10
	RAM_DATA_A<7..0>	4		200			167_MHZ	10 11
	RAM_DATA_B<7..0>	4		200			167_MHZ	10 11
	MEM_DQS<0>	4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200			167_MHZ	9 10
	RAM_DQS_A<0>	4		200			167_MHZ	10 11
	RAM_DQS_B<0>	4		200			167_MHZ	10 11
	MEM_DQM<0>	4		200			167_MHZ	9 10
	RAM_DQM_A<0>	4		200			167_MHZ	10 11
	RAM_DQM_B<0>	4		200			167_MHZ	10 11
GROUP 1	MEM_DATA<15..8>	4		200			167_MHZ	9 10
	RAM_DATA_A<15..8>	4		200			167_MHZ	10 11
	RAM_DATA_B<15..8>	4		200			167_MHZ	10 11
	MEM_DQS<1>	4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200			167_MHZ	9 10
	RAM_DQS_A<1>	4		200			167_MHZ	10 11
	RAM_DQS_B<1>	4		200			167_MHZ	10 11
	MEM_DQM<1>	4		200			167_MHZ	9 10
	RAM_DQM_A<1>	4		200			167_MHZ	10 11
	RAM_DQM_B<1>	4		200			167_MHZ	10 11
GROUP 2/3	MEM_DATA<31..16>	4		200			167_MHZ	9 10
	RAM_DATA_A<31..16>	4		200			167_MHZ	10 11
	RAM_DATA_B<31..16>	4		200			167_MHZ	10 11
	MEM_DQS<3..2>	4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200			167_MHZ	9 10
	RAM_DQS_A<3..2>	4		200			167_MHZ	10 11
DDR RAM	RAM_DQS_B<3..2>	4		200			167_MHZ	10 11
	MEM_DQM<3..2>	4		200			167_MHZ	9 10
	RAM_DQM_A<3..2>	4		200			167_MHZ	10 11
	RAM_DQM_B<3..2>	4		200			167_MHZ	10 11
GROUP 4/5	MEM_DATA<47..32>	4		200			167_MHZ	9 10
	RAM_DATA_A<47..32>	4		200			167_MHZ	10 11
	RAM_DATA_B<47..32>	4		200			167_MHZ	10 11
	MEM_DQS<5..4>	4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200			167_MHZ	9 10
	RAM_DQS_A<5..4>	4		200			167_MHZ	10 11
	RAM_DQS_B<5..4>	4		200			167_MHZ	10 11
	MEM_DQM<5..4>	4		200			167_MHZ	9 10
	RAM_DQM_A<5..4>	4		200			167_MHZ	10 11
	RAM_DQM_B<5..4>	4		200			167_MHZ	10 11
GROUP 6	MEM_DATA<55..48>	4		200			167_MHZ	9 10
	RAM_DATA_A<55..48>	4		200			167_MHZ	10 11
	RAM_DATA_B<55..48>	4		200			167_MHZ	10 11
	MEM_DQS<6>	4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200			167_MHZ	9 10
	RAM_DQS_A<6>	4		200			167_MHZ	10 11
	RAM_DQS_B<6>	4		200			167_MHZ	10 11
	MEM_DQM<6>	4		200			167_MHZ	9 10
	RAM_DQM_A<6>	4		200			167_MHZ	10 11
	RAM_DQM_B<6>	4		200			167_MHZ	10 11
GROUP 7	MEM_DATA<63..56>	4		200			167_MHZ	9 10
	RAM_DATA_A<63..56>	4		200			167_MHZ	10 11
	RAM_DATA_B<63..56>	4		200			167_MHZ	10 11
	MEM_DQS<7>	4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200			167_MHZ	9 10
	RAM_DQS_A<7>	4		200			167_MHZ	10 11
	RAM_DQS_B<7>	4		200			167_MHZ	10 11
	MEM_DQM<7>	4		200			167_MHZ	9 10
	RAM_DQM_A<7>	4		200			167_MHZ	10 11
	RAM_DQM_B<7>	4		200			167_MHZ	10 11
ADDR	MEM_ADDR<12..0>	4					83_MHZ	9
	RAM_ADDR<12..0>	6		200				9 11
	MEM_BA<1..0>	4						9
	RAM_BA<1..0>	6		200				9 11
CONTROL	MEM_CS_L<3..0>	4						9
	RAM_CS_L<3..0>	6		200				9 11
	MEM_CKE<3..0>	4						9
	RAM_CKE<3..0>	6		200				9 11
	MEM_RAS_L	4						9
	RAM_RAS_L	6		200.0000				9 11
	MEM_CAS_L	4						9
	RAM_CAS_L	6		200.0000				9 11
	MEM_WE_L	4						9
	RAM_WE_L	6		200.0000				9 11
	MEM_MUXSEL_H<1..0>	3						9 10
	MEM_MUXSEL_L<1..0>	3						9 10
	RAM_MUXSEL_H	5						10
	RAM_MUXSEL_L	5						10

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME			MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM	
INTREPID CLOCKS	SYSCLK_CPU_UF						10_MIL_SPACING	167.0 MHz:::	8
	SYSCLK_CPU			3	250.0000	200.0000	10_MIL_SPACING	167.0 MHz:::	5 8
	INT_CPUFB_OUT			3	250.0000		10_MIL_SPACING	167.0 MHz:::	8
	INT_CPUFB_OUT_SHORT			3	250.0000		10_MIL_SPACING	167.0 MHz:::	8
	INT_CPUFB_OUT_NORM			3	250.0000		10_MIL_SPACING	167.0 MHz:::	8
	INT_CPUFB_IN_NORM			3	250.0000		10_MIL_SPACING	167.0 MHz:::	8
	INT_CPUFB_LONG			3	250.0000		10_MIL_SPACING	167.0 MHz:::	8
	INT_CPUFB_IN			3	250.0000	200.0000	10_MIL_SPACING	167.0 MHz:::	8
	SYSCLK_DDRCLK_A0_UF			3	250.0000	200.0000	10_MIL_SPACING	167.0 MHz:::	9
	SYSCLK_DDRCLK_A0_L_UF			3	250.0000	200.0000	10_MIL_SPACING	167.0 MHz:::	9
	SYSCLK_DDRCLK_A1_UF			3	250.0000	200.0000	10_MIL_SPACING	167.0 MHz:::	9
	SYSCLK_DDRCLK_A1_L_UF			3	250.0000	200.0000	10_MIL_SPACING	167.0 MHz:::	9
	SYSCLK_DDRCLK_B0_UF			3	250.0000	200.0000	10_MIL_SPACING	167.0 MHz:::	9
	SYSCLK_DDRCLK_B0_L_UF			3	250.0000	200.0000	10_MIL_SPACING	167.0 MHz:::	9
	SYSCLK_DDRCLK_B1_UF			3	250.0000	200.0000	10_MIL_SPACING	167.0 MHz:::	9
	SYSCLK_DDRCLK_B1_L_UF			3	250.0000	200.0000	10_MIL_SPACING	167.0 MHz:::	9
	SYSCLK_DDRCLK_A0	DDRCLK_A0		3	250.0000	200.0000	10_MIL_SPACING	167.0 MHz:::	9 11
	SYSCLK_DDRCLK_A0_L	DDRCLK_A0		3	250.0000	200.0000	10_MIL_SPACING	167.0 MHz:::	9 11
	SYSCLK_DDRCLK_A1	DDRCLK_A1		3	250.0000	200.0000	10_MIL_SPACING	167.0 MHz:::	9 11
	SYSCLK_DDRCLK_A1_L	DDRCLK_A1		3	250.0000	200.0000	10_MIL_SPACING	167.0 MHz:::	9 11
	SYSCLK_DDRCLK_B0	DDRCLK_B0		3	250.0000	200.0000	10_MIL_SPACING	167.0 MHz:::	9 11
	SYSCLK_DDRCLK_B0_L	DDRCLK_B0		3	250.0000	200.0000	10_MIL_SPACING	167.0 MHz:::	9 11
	SYSCLK_DDRCLK_B1	DDRCLK_B1		3	250.0000	200.0000	10_MIL_SPACING	167.0 MHz:::	9 11
	SYSCLK_DDRCLK_B1_L	DDRCLK_B1		3	250.0000	200.0000	10_MIL_SPACING	167.0 MHz:::	9 11
	INT_REF_CLK_OUT			3	250.0000	200.0000	10_MIL_SPACING	49.92 MHz:::	14
	INT_REF_CLK_IN			4	250.0000	200.0000	10_MIL_SPACING	167.0 MHz:::	14
	CLK66M_GPU_AGP_UF					200.0000	10_MIL_SPACING	66.00 MHz:::	12
	CLK66M_GPU_AGP			4	400.0000	200.0000	10_MIL_SPACING	66.00 MHz:::	12 18
	INT_AGP_FB_OUT					200.0000	10_MIL_SPACING	66.00 MHz:::	12
	INT_AGP_FB_IN			4	500.0000	200.0000	10_MIL_SPACING	66.00 MHz:::	12
	CLK33M_CBUS_UF					200.0000	10_MIL_SPACING	33.00 MHz:::	12
	CLK33M_CBUS		SHOULD BE AT MOST 4 VIAS FOR CLK	6	500.0000	200.0000	10_MIL_SPACING	33.00 MHz:::	12 17
	CLK33M_AIRPORT_UF					200.0000	10_MIL_SPACING	33.00 MHz:::	12
	CLK33M_AIRPORT		SHOULD BE AT MOST 4 VIAS FOR CLK	6	500.0000	200.0000	10_MIL_SPACING	33.00 MHz:::	12 23 38
	CLK33M_USB2_UF					200.0000	10_MIL_SPACING	33.00 MHz:::	12
	CLK33M_USB2		SHOULD BE AT MOST 4 VIAS FOR CLK	6	500.0000	200.0000	10_MIL_SPACING	33.00 MHz:::	12 25
	INT_PCI_FB_OUT					200.0000	10_MIL_SPACING	33.00 MHz:::	12
	INT_PCI_FB_IN			3	500.0000	200.0000	10_MIL_SPACING	33.00 MHz:::	12
MAP31	GPU_CLK27M_OUT			3		200.0000	10_MIL_SPACING		20
	GPU_CLK27M_UF			3		200.0000	10_MIL_SPACING		20
	GPU_SSCLK_UF					200.0000	10_MIL_SPACING		20
	GPU_SSCLK_IN			3	500.0000	200.0000	10_MIL_SPACING		20
	GPU_FBCLK0			3		200.0000	10_MIL_SPACING		18
	GPU_FBCLK0_L			3		200.0000	10_MIL_SPACING		18
	GPU_FBCLK1			3		200.0000	10_MIL_SPACING		18
	GPU_FBCLK1_L			3		200.0000	10_MIL_SPACING		18
	GPU_DVO_CLKP			3	250.0000	200.0000	10_MIL_SPACING		20
CRYSTALS	CLK27M_GPU_XOUT						10_MIL_SPACING		20
	CLK27M_XTAL_IN						10_MIL_SPACING		20
	CLK27M_GPU_XIN						10_MIL_SPACING		20
	CLK18M_INT_XIN						10_MIL_SPACING		14
	CLK18M_INT_XOUT						10_MIL_SPACING		14
	CLK18M_XTAL_IN						10_MIL_SPACING		14
	CLK18M_INT_EXT						10_MIL_SPACING		14
	CLK25M_ENET_XIN						10_MIL_SPACING		26
	CLK25M_ENET_XOUT						10_MIL_SPACING		26
	NEC_XT1						10_MIL_SPACING		25
	NEC_XT2		THERE'S ANOTHER 280MIL LEG				10_MIL_SPACING		25
SOUND	SND_SCLK			5	500.0000	200.0000	10_MIL_SPACING		14 24 38
	SND_CLKOUT			5	500.0000	200.0000	10_MIL_SPACING		14 24 38
ETHERNET MARVELL	CLKENET_PHY_RX					200.0000		125.0 MHz:::	26
	CLKENET_LINK_RX			3	500.0000	200.0000	10_MIL_SPACING	125.0 MHz:::	13 26
	CLKENET_PHY_GBE_REF					200.0000		125.0 MHz:::	26
	CLKENET_LINK_GBE_REF			3	500.0000	200.0000	10_MIL_SPACING	125.0 MHz:::	13 26
	CLKENET_PHY_TX					200.0000		25.00 MHz:::	26
	CLKENET_LINK_TX			4	500.0000	200.0000	10_MIL_SPACING	25.00 MHz:::	13 26
	CLKENET_LINK_GTX					200.0000		125.0 MHz:::	13
	CLKENET_PHY_GTX			3	500.0000	200.0000	10_MIL_SPACING	125.0 MHz:::	13 26
FIREWIRE	CLKFW_PHY_PCLK					200.0000		49.15 MHz:::	27
	CLKFW_LINK_PCLK			3	500.0000	200.0000	10_MIL_SPACING	49.15 MHz:::	13 27
	CLKFW_PHY_LCLK			3	500.0000	200.0000	10_MIL_SPACING	49.15 MHz:::	13 27
	CLKFW_LINK_LCLK					200.0000		49.15 MHz:::	13
	FW_XI					200.0000	10_MIL_SPACING	98.03 MHz:::	27
	FW_OSC					200.0000	10_MIL_SPACING	98.03 MHz:::	27

SIGNAL CONSTRAINTS - PAGE 1

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SIZE	DRAWING NUMBER	REV.
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SCALE NONE	SHT 35 OF 43	

Digital Signals (cont'd)

GROUP	SIG_NAME	DELAY_RULE	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
AGP	AGP_AD<15..0>		5	100				66 MHZ	12 18
AGP BYTES 0-1	AGP_CBE<1..0>		5	100				66 MHZ	12 18
	AGP_AD_STB<0>		4	100	250	8 MIL SPACING		133 MHZ	12 18
	AGP_AD_STB_L<0>		4	100	250	8 MIL SPACING		133 MHZ	12 18
AGP BYTES 2-3	AGP_AD<31..16>		5	100				66 MHZ	12 18
	AGP_CBE<3..2>		5	100				66 MHZ	12 18
	AGP_AD_STB<1>		4	100	250	8 MIL SPACING		133 MHZ	12 18
	AGP_AD_STB_L<1>		4	100	250	8 MIL SPACING		133 MHZ	12 18
AGP SIDEBAND	AGP_SBA<7..0>		5	100				66 MHZ	12 18
	AGP_SB_STB		4	100.0000	350.0000	8 MIL SPACING		66.00 MHZ	12 18
	AGP_SB_STB_L		4	100.0000	350.0000	8 MIL SPACING		66.00 MHZ	12 18
AGP CONTROL	AGP_FRAME_L		6	250.0000				66.00 MHZ	12 18
	AGP_IRDY_L		6	250.0000				66.00 MHZ	12 18
	AGP_TRDY_L		6	250.0000				66.00 MHZ	12 18
	AGP_DEVSEL_L		6	250.0000				66.00 MHZ	12 18
	AGP_STOP_L		6	250.0000				66.00 MHZ	12 18
	AGP_PAR		6	250.0000				66.00 MHZ	12 18
	AGP_REQ_L		6	250.0000				66.00 MHZ	12 18
	AGP_GNT_L		6	250.0000				66.00 MHZ	12 18
	AGP_RBF_L		6	250.0000				66.00 MHZ	12 18
DVO	GPU_DVOD<0..11>		5	250					20
	GPU_DVO_HSYNC		5	250.0000					20
	GPU_DVO_VSYNC		5	250.0000					20
PCI	PCI_AD<31..0>					MIN_DAISY_CHAIN		33 MHZ	9 12 17 23 25 38
	PCI_CBE<3..0>					MIN_DAISY_CHAIN		33 MHZ	12 17 23 25 38
	PCI_FRAME_L					MIN_DAISY_CHAIN		33.00 MHZ	12 17 23 25 38
	PCI_IRDY_L					MIN_DAISY_CHAIN		33.00 MHZ	12 17 23 25 38
	PCI_TRDY_L					MIN_DAISY_CHAIN		33.00 MHZ	12 17 23 25 38
	PCI_DEVSEL_L					MIN_DAISY_CHAIN		33.00 MHZ	12 17 23 25 38
	PCI_STOP_L					MIN_DAISY_CHAIN		33.00 MHZ	12 17 23 25 38
	PCI_PAR					MIN_DAISY_CHAIN		33.00 MHZ	12 17 23 25 38
ULTRA ATA-100	UIDE_DATA<15..8>				200			100 MHZ	13 23
	UIDE_DATA<7>			NEED TO MATCH DELAY TO 250	200			100 MHZ	13 23
	UIDE_DATA<6..0>				200			100 MHZ	13 23
	UIDE_ADDR<2..0>				200			100 MHZ	13 23
	UIDE_RST_L				200.0000			100.0 MHZ	13 23
	UIDE_DIOW_L				200.0000			100.0 MHZ	13 23
	UIDE_DIOR_L			10 MIL SPACING	200.0000			100.0 MHZ	13 23
	UIDE_DMACK_L				200.0000			100.0 MHZ	13 23
	UIDE_CS0_L				200.0000			100.0 MHZ	13 23
	UIDE_CS1_L				200.0000			100.0 MHZ	13 23
	UIDE_DMARQ				200.0000			100.0 MHZ	13
	UIDE_IOCHRDY			10 MIL SPACING	200.0000			100.0 MHZ	13 23
	UIDE_INTRQ				200.0000			100.0 MHZ	13
	HD_DATA<15..0>		5		200			100 MHZ	23
	HD_ADDR<2..0>		5	TOTAL UIDE+HD SKEW <500MIL	200			100 MHZ	23
	HD_RESET_L		5		200.0000			100.0 MHZ	23
	HD_DIOW_L		5		200.0000			100.0 MHZ	23
	HD_DIOR_L		5	10 MIL SPACING	200.0000			100.0 MHZ	23
	HD_DMACK_L		5		200.0000			100.0 MHZ	23
	HD_CS0_L		5		200.0000			100.0 MHZ	23
	HD_CS1_L		5		200.0000			100.0 MHZ	23
	HD_DMARQ		5		200.0000			100.0 MHZ	13 23
	HD_IOCHRDY		5	10 MIL SPACING	200.0000			100.0 MHZ	23
	HD_INTRQ		5					100.0 MHZ	13 23
EIDE INTREPID	EIDE_DATA<15..0>							33 MHZ	13 23
	EIDE_ADDR<2..0>							33 MHZ	13 23
	EIDE_CS0_L							33.00 MHZ	13 23
	EIDE_CS1_L							33.00 MHZ	13 23
	EIDE_RD_L							33.00 MHZ	13 23
	EIDE_WR_L							33.00 MHZ	13 23
	EIDE_IOCHRDY							33.00 MHZ	13 23
	EIDE_INT							33.00 MHZ	13 23
	EIDE_RST_L							33.00 MHZ	13 23
	EIDE_DMACK_L							33.00 MHZ	13 23
	EIDE_DMARQ							33.00 MHZ	13 23
OPTICAL	EIDE_OPTICAL_DATA<15..0>							33 MHZ	23 38
	EIDE_OPTICAL_ADDR<2..0>							33 MHZ	23 38
	EIDE_OPTICAL_CS0_L							33.00 MHZ	23 38
	EIDE_OPTICAL_CS1_L							33.00 MHZ	23 38
	EIDE_OPTICAL_RD_L							33.00 MHZ	23 38
	EIDE_OPTICAL_WR_L							33.00 MHZ	23 38
	EIDE_OPTICAL_IOCHRDY							33.00 MHZ	23 38
	EIDE_OPTICAL_INT							33.00 MHZ	23 38
	EIDE_OPTICAL_RST_L							33.00 MHZ	23 38
	EIDE_OPTICAL_DMAACK_L							33.00 MHZ	23 38
	EIDE_OPTICAL_DMA_RQ							33.00 MHZ	23 38
ETHERNET MII	ENET_LINK_RXD<7..0>		5						13 26
	ENET_RX_DV								13 26
	ENET_RX_ER								13 26
	ENET_PHY_TXD<7..0>		5						13 26
	ENET_LINK_TXD<7..0>								13
	ENET_PHY_TX_ER		5						13 26
	ENET_LINK_TX_ER								13
	ENET_PHY_TX_EN		5						13 26
	ENET_LINK_TX_EN								13
	ENET_MDIO								13 26
	ENET_MDC								13 26
	ENET_COL								13 26
	ENET_CRS								13 26
FIREWIRE MII	FW_LINK_DATA<7..0>		5						13 27
	FW_PHY_DATA<7..0>		5						27
	FW_LINK_CNTL<1..0>								13 27
	FW_PHY_CNTL<1..0>								27
	FW_LINK_LREQ								13
	FW_PHY_LREQ								13 27
	FW_PINT								13 27

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR		MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS	
ETHERNET	MDI_M<0>	ENET_MDI0					26
	MDI_P<0>	ENET_MDI0					26
	MDI_M<1>	ENET_MDI1		SPACING DELETED BECAUSE			26
	MDI_P<1>	ENET_MDI1		OF PHYSICAL CONSTRAINTS			26
	MDI_M<2>	ENET_MDI2		AROUND MARVELL PHY			26
	MDI_P<2>	ENET_MDI2					26
	MDI_M<3>	ENET_MDI3					26
	MDI_P<3>	ENET_MDI3					26
	RJ45_DN<0>	RJ45_DP0			10 MIL SPACING		26 38
	RJ45_DP<0>	RJ45_DP0			10 MIL SPACING		26 38
	RJ45_DN<1>	RJ45_DP1			10 MIL SPACING		26 38
	RJ45_DP<1>	RJ45_DP1			10 MIL SPACING		26 38
	RJ45_DN<2>	RJ45_DP2			10 MIL SPACING		26 38
	RJ45_DP<2>	RJ45_DP2			10 MIL SPACING		26 38
	RJ45_DN<3>	RJ45_DP3			10 MIL SPACING		26 38
	RJ45_DP<3>	RJ45_DP3			10 MIL SPACING		26 38
FIREWIRE	FW_TPA0N	FW_TPA0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		27 28
	FW_TPA0P	FW_TPA0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		27 28
	FW_TPB0N	FW_TPB0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		27 28
	FW_TPB0P	FW_TPB0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		27 28
	FW_TPI0N	FW_TPI0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPI0P	FW_TPI0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPO0N	FW_TPO0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPO0P	FW_TPO0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPA1N	FW_TPA1		500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		27 28
	FW_TPA1P	FW_TPA1		500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		27 28
	FW_TPB1N	FW_TPB1		500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		27 28
	FW_TPB1P	FW_TPB1		500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		27 28
	FW_TPI1N	FW_TPI1			MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 38
	FW_TPI1P	FW_TPI1			MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 38
	FW_TPO1N	FW_TPO1			MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 38
	FW_TPO1P	FW_TPO1			MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 38
LVDS LOWER	CLKLVDS_LN	CLKLVDS_L		500.0000	10 MIL SPACING	4	19 21 38
	CLKLVDS_LP	CLKLVDS_L		500.0000	10 MIL SPACING	4	19 21 38
	LVDS_L0N	LVDS_L0			10 MIL SPACING		19 21 38
	LVDS_L0P	LVDS_L0			10 MIL SPACING		19 21 38
	LVDS_L1N	LVDS_L1			10 MIL SPACING		19 21 38
	LVDS_L1P	LVDS_L1			10 MIL SPACING		19 21 38
	LVDS_L2N	LVDS_L2			10 MIL SPACING		19 21 38
	LVDS_L2P	LVDS_L2			10 MIL SPACING		19 21 38
UPPER	CLKLVDS_UN	CLKLVDS_U		500.0000	10 MIL SPACING	4	19 21 38
	CLKLVDS_UP	CLKLVDS_U		500.0000	10 MIL SPACING	4	19 21 38
	LVDS_U0N	LVDS_U0			10 MIL SPACING		19 21 38
	LVDS_U0P	LVDS_U0			10 MIL SPACING		19 21 38
	LVDS_U1N	LVDS_U1			10 MIL SPACING		19 21 38
	LVDS_U1P	LVDS_U1			10 MIL SPACING		19 21 38
	LVDS_U2N	LVDS_U2			10 MIL SPACING		19 21 38
	LVDS_U2P	LVDS_U2			10 MIL SPACING		19 21 38
TMDS	TMDS_CONN_CLKN	CLKCONN_TMDS		500.0000	10 MIL SPACING	4	21 38
	TMDS_CONN_CLKP	CLKCONN_TMDS		500.0000	10 MIL SPACING	4	21 38
	TMDS_CLKN	CLKTMDS		500.0000	10 MIL SPACING	4	19 20 21
	TMDS_CLKP	CLKTMDS		500.0000	10 MIL SPACING	4	19 20 21
	TMDS_DN<0>	TMDS_D0			10 MIL SPACING		19 20 21 38
	TMDS_DP<0>	TMDS_D0			10 MIL SPACING		19 20 21 38
	TMDS_DN<1>	TMDS_D1			10 MIL SPACING		19 20 21 38
	TMDS_DP<1>	TMDS_D1			10 MIL SPACING		19 20 21 38
	TMDS_DN<2>	TMDS_D2			10 MIL SPACING		19 20 21 38
	TMDS_DP<2>	TMDS_D2			10 MIL SPACING		19 20 21 38
USB	NEC_USB_DAM	NEC_USB_DA		MIN_LINE_WIDTH=5	10 MIL SPACING		25
	NEC_USB_DAP	NEC_USB_DA		MIN_LINE_WIDTH=5	10 MIL SPACING		25
	USB_DEM	USB_DE			5 MIL SPACING		14
	USB_DEP	USB_DE			5 MIL SPACING		14
	NEC_USB_DBM	NEC_USB_DB		MIN_LINE_WIDTH=5	10 MIL SPACING		25
	NEC_USB_DBP	NEC_USB_DB		MIN_LINE_WIDTH=5	10 MIL SPACING		25
	USB_DFM	USB_DF			5 MIL SPACING		14
	USB_DFP	USB_DF			5 MIL SPACING		14
	BT_USB_DM	BT_USB_D			5 MIL SPACING		14 23 38
	BT_USB_DP	BT_USB_D			5 MIL SPACING		14 23 38
	NEC_USB_RSDM1	NEC_USB_RSD1		MIN_LINE_WIDTH=5	10 MIL SPACING		25
	NEC_USB_RSDP1	NEC_USB_RSD1		MIN_LINE_WIDTH=5	10 MIL SPACING		25
	NEC_USB_RSDM2	NEC_USB_RSD2		MIN_LINE_WIDTH=5	10 MIL SPACING		25
	NEC_USB_RSDP2	NEC_USB_RSD2		MIN_LINE_WIDTH=5	10 MIL SPACING		25
	MODEM_USB_DM	MODEM_USB_D			5 MIL SPACING		14 24 38
	MODEM_USB_DP	MODEM_USB_D			5 MIL SPACING		14 24 38
	LEFT_USB_DM	LEFT_USB		MIN_LINE_WIDTH=5	10 MIL SPACING		23 25 38
	LEFT_USB_DP	LEFT_USB		MIN_LINE_WIDTH=5	10 MIL SPACING		23 25 38
	RIGHT_USB_DM	RIGHT_USB		MIN_LINE_WIDTH=5	10 MIL SPACING		25 31 38
	RIGHT_USB_DP	RIGHT_USB		MIN_LINE_WIDTH=5	10 MIL SPACING		25 31 38
POWER SUPPLIES	1772_CSSN	1772_CSS					30
	1772_CSSP	1772_CSS					30
	1772_CSIN	1772_CSI					30
	1772_CSIP	1772_CSI					30
	3V_SNSM	3V_SNS					32
	3V_SNSP	3V_SNS					32
	5V_SNSM	5V_SNS					32
	5V_SNSP	5V_SNS					32
THERMOSTAT	THERM1_DM	THERM1					24
	THERM1_DP	THERM1					24
	THERM2_DM	THERM2					24
	THERM2_DP	THERM2					24
	THERM1_M_DM	THERM1_MAIN					24
	THERM1_M_DP	THERM1_MAIN					24
	THERM2_M_DM	THERM2_MAIN					24
	THERM2_M_DP	THERM2_MAIN					24
	THERM1_A_DM	THERM1_ALT					24
	THERM1_A_DP	THERM1_ALT					24
	THERM2_A_DM	THERM2_ALT					24
	THERM2_A_DP	THERM2_ALT					24

INTERNAL LAYER
ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.57OHM
ZDIFF = 99.8OHM

FOR FIREWIRE
ER = 4.3 (DIELECTRIC CONSTANT)
W = 3.4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 53.37OHM
ZDIFF = 107.17OHM

INTERNAL LAYER (USB1.1/USB 2.0)
ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL(USB 1.1)/ 5MIL(USB 2.0) (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 5MIL (USB 1.1) (SEPERATION OF DIFF TRACES)
S = 10MIL (USB 2.0) (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.5OHM (USB 1.1)/ 46.2OHM (USB 2.0)
ZDIFF = 89.3OHM (USB 1.1)/ 89.4OHM (USB 2.0)

SIGNAL CONSTRAINTS - PAGE 2

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SCALE NONE	SHT 36 OF 43	

POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	38
	+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	38
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	38
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	38
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18 34
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	34
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30 31
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30 38
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30 38
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		30
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	30
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		30
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		30
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10		30
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		29 31
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10		31 32
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		31
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		31
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		29
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23 32
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23
TRACKPAD	+5V_TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10		22 38
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		22 38
VIDEO	+12_8V_INV	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21 38
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21 38
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21 38
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	21
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		21
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		21
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		21 38
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		21 38
KB LED	KBD_LED1_OUT	VOLTAGE=0V	MIN_LINE_WIDTH=10		22 38
	KBD_LED2_OUT	VOLTAGE=0V	MIN_LINE_WIDTH=10		22 38
FAN GND	FAN1_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24 38
	FAN2_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24 38
SOUND	+5V_SOUND_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24
	SND_AGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=15	24

	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	GND	
I/O AREA	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND1	
	CHGND1				
INVERTER	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND2	
	CHGND2				
TRACKPAD	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND3	
	CHGND3				
LVDS	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND4	
	CHGND4				
I/O AREA	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND5	
	CHGND5				
I/O AREA	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND6	
	CHGND6				
ENET_CTAP_CHGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12		26

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 33 38
	CPU_AVDD	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 7 8 15 16 22 33
L3 CACHE	L3_VREF	VOLTAGE=0.75V	MIN_LINE_WIDTH=10		
	L3_CLK_REF	VOLTAGE=0.75V	MIN_LINE_WIDTH=10		
	L3_OVDD	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
DDR RAM	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		11
INTREPID	+2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	9 10 15 16
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
PLLS	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	8 12 14
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	14
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	12
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	8
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
			MIN_NECK_WIDTH REDUCED FOR TESTPOINTS		
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		9
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		12
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10		9
	UIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8		13
CARDBUS	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
NVIDIA NV17MAP	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	19 38
	+2_5V_GPU_FB	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 14 18 19 20
	+3V_GPU_DVO	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	20
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 15 16 18 19
	+3V_DAC1VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	20
	+3V_DAC2VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	20
	+3V_GPU_AVDD1	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	+3V_GPU_AVDD0	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	+3V_GPU_PLLVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	20
	+3V_GPU_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	20
	+2_8V_IFP_PLLVDD	VOLTAGE=2.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
	GPU_AGP_VREF	VOLTAGE=0.75V	MIN_LINE_WIDTH=10		18
	GPU_FB_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		18
SILICON IMAGE	+3V_SI_PLLVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
	+3V_SI_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
	+3V_SI_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
88E1111	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	26
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	26
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	26
FW	LM2594_IN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_ESD_ILIM	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_ESD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+FW_FUSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	27 28
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	+FW_PWR_PORTA	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27 28
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	27
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	FW_TPO0R	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28 38
USB 2.0	NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25
	+3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25
INTREPID SSCG	+3V_CG_PLL_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	14
	+2_5V_CG_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	14

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	1625_VSW	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		31
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		31
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		31
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	30 31
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	32
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		32
MAX1715 2.5V SWITCHER	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	34
	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
1.5V SWITCHER	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8		34
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	34
	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
CONTROL	1_5V_ILIM		MIN_LINE_WIDTH=8		34
	2_5V_ILIM		MIN_LINE_WIDTH=8		34
	MAX1715_TON		MIN_LINE_WIDTH=8		34
	MAX1715_SKIP		MIN_LINE_WIDTH=8		34
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8		34
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	33
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10	33
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	33
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	33
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	33
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	33
	VCORE_ILIM		MIN_LINE_WIDTH=8		33
	VCORE_REF		MIN_LINE_WIDTH=8		33
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8		33
	VCORE_CC		MIN_LINE_WIDTH=8		33
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		33 38
	VCORE_TIME		MIN_LINE_WIDTH=8		33
	VCORE_VGATE		MIN_LINE_WIDTH=8		14 33
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30		33
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8		33
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		33
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8		33
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	19
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	19
	1778_ION		MIN_LINE_WIDTH=8		19
	1778_ITH		MIN_LINE_WIDTH=8		19
	1778_ITH_RC		MIN_LINE_WIDTH=8		19
	1_5V_2_5V_OK		MIN_LINE_WIDTH=8		19 34
	1778_VFB		MIN_LINE_WIDTH=8		19
	1778_FCB		MIN_LINE_WIDTH=8		19
	1778_VRNG		MIN_LINE_WIDTH=8		19
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
	1_8V_VFB		MIN_LINE_WIDTH=8		34
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8		34
	LTC3411_ITH		MIN_LINE_WIDTH=8		34
	LTC3411_SYNC		MIN_LINE_WIDTH=8		34
	LTC3411_SHDN		MIN_LINE_WIDTH=8		34
LTC1962 INT PLLS	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	14
	LTC1962_L3_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_L3_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_1V5_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_1V5_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	

SIGNAL CONSTRAINTS - PAGE 3

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SIZE	DRAWING NUMBER	REV.
D	051-6443	03
SCALE NONE	SHT 37 OF 43	

FUNCTIONAL TEST POINTS

FUNC_TEST=YES
JTAG_ASIC_TMS 13 26

FUNC_TEST=YES
JTAG_ASIC_TDI 13

FUNC_TEST=YES
JTAG_ASIC_TDO_TP 26

FUNC_TEST=YES
JTAG_ASIC_TCK 13 26

FUNC_TEST=YES
JTAG_ASIC_TRST_L 13 26

FUNC_TEST=YES
CPU_CHKSTP_OUT_L 5

FUNC_TEST=YES
CPU_SRESET_L 5

FUNC_TEST=YES
CPU_HRESET_L 5 7 22

FUNC_TEST=YES
JTAG_CPU_TMS 5 22

FUNC_TEST=YES
JTAG_CPU_TDI 5 22

FUNC_TEST=YES
JTAG_CPU_TDO_TP 5

FUNC_TEST=YES
JTAG_CPU_TCK 5 22

FUNC_TEST=YES
JTAG_CPU_TRST_L 5 22

FUNC_TEST=YES
INT_I2C_CLK0 11 13 22

FUNC_TEST=YES
INT_I2C_DATA0 11 13 22

FUNC_TEST=YES
INT_I2C_CLK1 13 14 19 24

FUNC_TEST=YES
INT_I2C_DATA1 13 14 19 24

FUNC_TEST=YES
CBUS_DET_1_L 17

FUNC_TEST=YES
CBUS_DET_2_L 17

FUNC_TEST=TRUE
TMDS_DN<0> 19 20 21 36

FUNC_TEST=TRUE
TMDS_DP<0> 19 20 21 36

FUNC_TEST=TRUE
TMDS_DN<1> 19 20 21 36

FUNC_TEST=TRUE
TMDS_DP<1> 19 20 21 36

FUNC_TEST=TRUE
TMDS_DN<2> 19 20 21 36

FUNC_TEST=TRUE
TMDS_DP<2> 19 20 21 36

FUNC_TEST=YES
TMDS_CONN_CLKN 21 36

FUNC_TEST=YES
TMDS_CONN_CLKP 21 36

FUNC_TEST=YES
VGA_R 21

FUNC_TEST=YES
VGA_G 21

FUNC_TEST=YES
VGA_B 21

FUNC_TEST=YES
VGA_VSYNC 20 21

FUNC_TEST=YES
VGA_HSYNC 20 21

FUNC_TEST=YES
DVI_DDC_CLK_UF 21

FUNC_TEST=YES
DVI_DDC_DATA_UF 21

FUNC_TEST=YES
DVI_HPD_UF 21

FUNC_TEST=YES
LVDS_L0N 19 21 36

FUNC_TEST=YES
LVDS_L0P 19 21 36

FUNC_TEST=YES
LVDS_L1N 19 21 36

FUNC_TEST=YES
LVDS_L1P 19 21 36

FUNC_TEST=YES
LVDS_L2N 19 21 36

FUNC_TEST=YES
LVDS_L2P 19 21 36

FUNC_TEST=YES
CLKLVDS_LN 19 21 36

FUNC_TEST=YES
CLKLVDS_LP 19 21 36

FUNC_TEST=YES
LVDS_U0N 19 21 36

FUNC_TEST=YES
LVDS_U0P 19 21 36

FUNC_TEST=YES
LVDS_U1N 19 21 36

FUNC_TEST=YES
LVDS_U1P 19 21 36

FUNC_TEST=YES
LVDS_U2N 19 21 36

FUNC_TEST=YES
LVDS_U2P 19 21 36

FUNC_TEST=YES
CLKLVDS_UN 19 21 36

FUNC_TEST=YES
CLKLVDS_UP 19 21 36

FUNC_TEST=YES
LVDS_DDC_CLK 19 21

FUNC_TEST=YES
LVDS_DDC_DATA 19 21

FUNC_TEST=YES
BRIGHT_PWM 21

FUNC_TEST=YES
TV_GND1 21 37

FUNC_TEST=YES
TV_GND2 21 37

FUNC_TEST=YES
TV_C 21

FUNC_TEST=YES
TV_Y 21

FUNC_TEST=YES
TV_COMP 21

FUNC_TEST=YES
SND_TO_AUDIO 14 24

FUNC_TEST=YES
SND_SYNC 14 24

FUNC_TEST=YES
SND_CLKOUT 14 24 35

FUNC_TEST=YES
SND_HP_MUTE_L 14 24

FUNC_TEST=YES
SND_AMP_MUTE_L 14 24

FUNC_TEST=YES
INT_AUDIO_TO_SND 14 24

FUNC_TEST=YES
SND_SCLK 14 24 35

FUNC_TEST=YES
SND_HW_RESET_L 14 24

FUNC_TEST=YES
SND_HP_SENSE_L 14 24

FUNC_TEST=YES
SND_LIN_SENSE_L 14 24

FUNC_TEST=YES
INT_I2C_DATA2 14 24

FUNC_TEST=YES
INT_I2C_CLK2 14 24

FUNC_TEST=YES
USB_D1M 14 25

FUNC_TEST=YES
USB_D1P 14 25

NO LONGER NEED BY TEST GROUP
FUNC_TEST=YES
USB_D2M 14 25

FUNC_TEST=YES
USB_D2P 14 25

FUNC_TEST=YES
BT_USB_DM 14 23 36

FUNC_TEST=YES
BT_USB_DP 14 23 36

FUNC_TEST=YES
MODEM_USB_DM 14 24 36

FUNC_TEST=YES
MODEM_USB_DP 14 24 36

FUNC_TEST=TRUE
PCI_AD<0> 9 12 17 23 25 36

FUNC_TEST=TRUE
PCI_AD<1> 9 12 17 23 25 36

FUNC_TEST=TRUE
PCI_AD<2> 9 12 17 23 25 36

FUNC_TEST=TRUE
PCI_AD<3> 9 12 17 23 25 36

FUNC_TEST=TRUE
PCI_AD<4> 9 12 17 23 25 36

FUNC_TEST=TRUE
PCI_AD<5> 9 12 17 23 25 36

FUNC_TEST=TRUE
PCI_AD<6> 9 12 17 23 25 36

FUNC_TEST=TRUE
PCI_AD<7> 9 12 17 23 25 36

FUNC_TEST=TRUE
PCI_AD<8> 9 12 17 23 25 36

FUNC_TEST=TRUE
PCI_AD<9> 9 12 17 23 25 36

FUNC_TEST=TRUE
PCI_AD<10> 9 12 17 23 25 36

FUNC_TEST=TRUE
PCI_AD<11> 9 12 17 23 25 36

FUNC_TEST=TRUE
PCI_AD<12> 9 12 17 23 25 36

FUNC_TEST=TRUE
PCI_AD<13> 9 12 17 23 25 36

FUNC_TEST=TRUE
PCI_AD<14> 9 12 17 23 25 36

FUNC_TEST=TRUE
PCI_AD<15> 9 12 17 23 25 36

FUNC_TEST=TRUE
PCI_AD<16> 9 12 17 23 25 36

FUNC_TEST=TRUE
PCI_AD<17> 9 12 17 23 25 36

FUNC_TEST=TRUE
PCI_AD<18> 9 12 17 23 25 36

FUNC_TEST=TRUE
PCI_AD<19> 9 12 17 23 25 36

FUNC_TEST=TRUE
PCI_AD<20> 9 12 17 23 25 36

FUNC_TEST=TRUE
PCI_AD<21> 12 17 23 25 36

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PCI_AD<22> 12 17 23 25 36

FUNC_TEST=TRUE
PCI_AD<23> 12 17 23 25 36

FUNC_TEST=TRUE
PCI_AD<24> 9 12 17 23 25 36

FUNC_TEST=TRUE
PCI_AD<25> 9 12 17 23 25 36

FUNC_TEST=TRUE
PCI_AD<26> 9 12 17 23 25 36

FUNC_TEST=TRUE
PCI_AD<27> 9 12 17 23 25 36

FUNC_TEST=TRUE
PCI_AD<28> 9 12 17 23 25 36

FUNC_TEST=TRUE
PCI_AD<29> 9 12 17 23 25 36

FUNC_TEST=TRUE
PCI_AD<30> 9 12 17 23 25 36

FUNC_TEST=TRUE
PCI_AD<31> 9 12 17 23 25 36

FUNC_TEST=YES
PCI_FRAME_L 12 17 23 25 36

FUNC_TEST=YES
PCI_TRDY_L 12 17 23 25 36

FUNC_TEST=YES
PCI_IRDY_L 12 17 23 25 36

FUNC_TEST=YES
PCI_DEVSEL_L 12 17 23 25 36

FUNC_TEST=YES
PCI_STOP_L 12 17 23 25 36

FUNC_TEST=YES
PCI_PAR 12 17 23 25 36

FUNC_TEST=TRUE
PCI_CBE<0> 12 17 23 25 36

FUNC_TEST=TRUE
PCI_CBE<1> 12 17 23 25 36

FUNC_TEST=TRUE
PCI_CBE<2> 12 17 23 25 36

FUNC_TEST=TRUE
PCI_CBE<3> 12 17 23 25 36

FUNC_TEST=YES
AIRPORT_PCI_REQ_L 12 23

FUNC_TEST=YES
AIRPORT_PCI_GNT_L 12 23

FUNC_TEST=YES
AIRPORT_PCI_INT_L 14 23

FUNC_TEST=TRUE
EIDE_OPTICAL_DATA<0> 23 36

FUNC_TEST=TRUE
EIDE_OPTICAL_DATA<1> 23 36

FUNC_TEST=TRUE
EIDE_OPTICAL_DATA<2> 23 36

FUNC_TEST=TRUE
EIDE_OPTICAL_DATA<3> 23 36

FUNC_TEST=TRUE
EIDE_OPTICAL_DATA<4> 23 36

FUNC_TEST=TRUE
EIDE_OPTICAL_DATA<5> 23 36

FUNC_TEST=TRUE
EIDE_OPTICAL_DATA<6> 23 36

FUNC_TEST=TRUE
EIDE_OPTICAL_DATA<7> 23 36

FUNC_TEST=TRUE
EIDE_OPTICAL_DATA<8> 23 36

FUNC_TEST=TRUE
EIDE_OPTICAL_DATA<9> 23 36

FUNC_TEST=TRUE
EIDE_OPTICAL_DATA<10> 23 36

FUNC_TEST=TRUE
EIDE_OPTICAL_DATA<11> 23 36

FUNC_TEST=TRUE
EIDE_OPTICAL_DATA<12> 23 36

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EIDE_OPTICAL_DATA<13> 23 36

FUNC_TEST=TRUE
EIDE_OPTICAL_DATA<14> 23 36

FUNC_TEST=TRUE
EIDE_OPTICAL_DATA<15> 23 36

FUNC_TEST=YES
EIDE_OPTICAL_DMA_RQ 23 36

FUNC_TEST=YES
EIDE_OPTICAL_RD_L 23 36

FUNC_TEST=YES
EIDE_OPTICAL_DMAACK_L 23 36

FUNC_TEST=TRUE
EIDE_OPTICAL_ADDR<0> 23 36

FUNC_TEST=TRUE
EIDE_OPTICAL_ADDR<1> 23 36

FUNC_TEST=TRUE
EIDE_OPTICAL_ADDR<2> 23 36

FUNC_TEST=YES
EIDE_OPTICAL_CS0_L 23 36

FUNC_TEST=YES
EIDE_OPTICAL_CS1_L 23 36

FUNC_TEST=YES
EIDE_OPTICAL_RST_L 23 36

FUNC_TEST=YES
EIDE_OPTICAL_WR_L 23 36

FUNC_TEST=YES
EIDE_OPTICAL_IOCHRDY 23 36

FUNC_TEST=YES
EIDE_OPTICAL_INT 23 36

FUNC_TEST=YES
TPAD_F_TXD 22

FUNC_TEST=YES
TPAD_F_RXD 22

FUNC_TEST=YES
LID_CLOSED_L 22

FUNC_TEST=YES
COMM_RESET_L 14 24

FUNC_TEST=YES
COMM_SHUTDOWN 14 24

FUNC_TEST=YES
COMM_RING_DET_L 14 24 29

FUNC_TEST=YES
KBD_ID 22 29

FUNC_TEST=YES
+5V_TPAD_SLEEP 22 37

FUNC_TEST=YES
+3V_HALL_EFFECT 22 37

FUNC_TEST=YES
KBD_CAPSLOCK_LED 22

FUNC_TEST=YES
KBD_FUNCTION_L 22 29

FUNC_TEST=YES
KBD_CONTROL_L 22 29

FUNC_TEST=YES
KBD_COMMAND_L 22 29

FUNC_TEST=YES
KBD_OPTION_L 22 29

FUNC_TEST=YES
KBD_SHIFT_L 22 29

FUNC_TEST=TRUE
KBD_X<0> 22 29

FUNC_TEST=TRUE
KBD_X<1> 22 29

FUNC_TEST=TRUE
KBD_X<2> 22 29

FUNC_TEST=TRUE
KBD_X<3> 22 29

FUNC_TEST=TRUE
KBD_X<4> 22 29

FUNC_TEST=TRUE
KBD_X<5> 22 29

FUNC_TEST=TRUE
KBD_X<6> 22 29

FUNC_TEST=TRUE
KBD_X<7> 22 29

FUNC_TEST=TRUE
KBD_X<8> 22 29

FUNC_TEST=TRUE
KBD_X<9> 22 29

FUNC_TEST=TRUE
KBD_Y<0> 22 29

FUNC_TEST=TRUE
KBD_Y<1> 22 29

FUNC_TEST=TRUE
KBD_Y<2> 22 29

FUNC_TEST=TRUE
KBD_Y<3> 22 29

FUNC_TEST=TRUE
KBD_Y<4> 22 29

FUNC_TEST=TRUE
KBD_Y<5> 22 29

FUNC_TEST=TRUE
KBD_Y<6> 22 29

FUNC_TEST=TRUE
KBD_Y<7> 22 29

FUNC_TEST=YES
KBD_NUMLOCK_LED 22

FUNC_TEST=YES
+BATT_POS 30 37

FUNC_TEST=YES
BATT_CLK 30

FUNC_TEST=YES
BATT_DATA 30

FUNC_TEST=YES
BATT_NEG 30 37

FUNC_TEST=YES
PMU_BATT_DET_L 29 30

FUNC_TEST=YES
FAN1_GND 24 37

FUNC_TEST=YES
FAN1_TACH 24

FUNC_TEST=YES
FAN2_GND 24 37

FUNC_TEST=YES
FAN2_TACH 24

FUNC_TEST=TRUE
RJ45_DP<0> 26 36

FUNC_TEST=TRUE
RJ45_DN<0> 26 36

FUNC_TEST=TRUE
RJ45_DP<1> 26 36

FUNC_TEST=TRUE
RJ45_DN<1> 26 36

FUNC_TEST=TRUE
RJ45_DP<2> 26 36

FUNC_TEST=TRUE
RJ45_DN<2> 26 36

FUNC_TEST=TRUE
RJ45_DP<3> 26 36

FUNC_TEST=TRUE
RJ45_DN<3> 26 36

FUNC_TEST=YES
FW_TPO0R 28 37

FUNC_TEST=YES
FW_TPO1P 28 36

FUNC_TEST=YES
FW_TPO1N 28 36

FUNC_TEST=YES
FW_TPI1P 28 36

FUNC_TEST=YES
FW_TPI1N 28 36

FUNC_TEST=YES
CHARGE_LED_L 29 30

FUNC_TEST=YES
ADAPTER_DET 29 30

FUNC_TEST=YES
SUTRO_ALS_GAIN_SW 22 23

FUNC_TEST=YES
SUTRO_ALS_OUT 22 23

FUNC_TEST=YES
KBD_LED1_OUT 22 37

FUNC_TEST=YES
KBD_LED2_OUT 22 37

FUNC_TEST=YES
COMM_TXD_L 14 24

FUNC_TEST=YES
COMM_TRXC 14 24

FUNC_TEST=YES
COMM_GPIO_L 14 24

FUNC_TEST=YES
COMM_DTR_L 14 24

FUNC_TEST=YES
COMM_RTS_L 14 24

FUNC_TEST=YES
COMM_RXD 14 24

FUNC_TEST=YES
PMU_KB_RESET_L 29

FUNC_TEST=YES
PWR_BUTTON_L 22 24

FUNC_TEST=TRUE
+PBUS 37

FUNC_TEST=TRUE
+24V_PBUS 37

FUNC_TEST=YES
GPU_VCORE 19 37

FUNC_TEST=YES
CPU_VCORE_SLEEP 5 33 37

FUNC_TEST=YES
VCORE_FB 33 37

FUNC_TEST=TRUE
+1_8V_MAIN 37

FUNC_TEST=TRUE
+3V_PMU 37

FUNC_TEST=YES
+5V_DDC_SLEEP 21 37

FUNC_TEST=YES
+12_8V_INV 21 37

FUNC_TEST=YES
+5V_INV_SW 21 37

FUNC_TEST=YES
LEFT_USB_DM 23 25 36

FUNC_TEST=YES
LEFT_USB_DP 23 25 36

FUNC_TEST=YES
RIGHT_USB_DM 25 31 36

FUNC_TEST=YES
RIGHT_USB_DP 25 31 36

FUNC_TEST=YES
NEC_LEFT_USB_PWREN 23 25

FUNC_TEST=YES
NEC_LEFT_USB_OVERCURRENT 23 25

FUNC_TEST=YES
NEC_RIGHT_USB_PWREN 25 31

FUNC_TEST=YES
NEC_RIGHT_USB_OVERCURRENT 25 31

FUNC_TEST=YES
DCDC_EN 19 28 31 32 33

FUNC_TEST=YES
BBANG_HRESET_L 22

FUNC_TEST=YES
LT1962_L3_ADJ

FUNC_TEST=YES
MAIN_RESET_L 14 17 18 20 23 25 29

FUNC_TEST=YES
RF_DISABLE_L_SPN 23

FUNC_TEST=YES
AIRPORT_CLKRUN_L 23

FUNC_TEST=YES
ROM_RW_L 9 12 23

FUNC_TEST=YES
ROM_ONBOARD_CS_L 9 23

FUNC_TEST=YES
ROM_CS_L 9 12 23

FUNC_TEST=YES
CLK33M_AIRPORT 12 23 35

FUNC_TEST=YES
AIRPORT_IDSEL 23

FUNC_TEST=YES
ROM_OE_L 9 12 23

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SIZE	DRAWING NUMBER	REV.
D	051-6443	03
SCALE NONE	SHT 38 OF 43	

REVISION HISTORY

REV 0.01 - 03/06/2003

3/3
1) Initial check-in of Enterprise schematic after conversion to Concept 14.2

3/10
2) added 8 new 10uF vcore caps
3) added jumpers at 1.5V, 1.8V, 2.5V, 3.3V, 5V, and PBUS supply outputs
4) added 8 more 0.1uF vcore byapass caps

3/11
5) removed dedicated boot banger circuit (U5400,U5200,RP46,U9,U1000)
6) updated firewire to phy to rev A prt number
7) changed cpu PLL config to 1083/833
8) changed reset to U56 (clock slewing chip) to MAIN_RESET_L
9) changed C550 to 138S0536 to limit AVL
10) changed Vcore stuffing options to 1.4V/1.025V using analog mux to support slewing
11) changed stuffing to set Vcore offset to 0mV by default
12) changed comments to eliminate references to L3 in power supply section

3/18
13) changed stuffing options for GPU PCI ID to 0x319
14) changed R164 (DAC1RSET) to 107 ohm pulldown
15) added 10K pulldown to U43 pin A21
16) changed fan controller to ADT7460

3/19
17) added pads for 0.1uF cap from +Adapter to digital gnd for EMC
18) added pads for 0 ohm between chassis and digital gnd near ENET connector for EMC
19) corrected path to correct for last checkin
20) removed BOM table for MAP31
21) REMOVED ALL RELATIVE_PROPAGATION_DELAY AND PROPAGATION_DELAY PROPERTIES TO PRERPARE FOR CONSTRAINT BACK ANNOTATION
23) ***BOARD RENUMBERED***
22) changed CHGND on R616 to CHGND1

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SIZE	DRAWING NUMBER	REV.
D	051-6443	03
SCALE NONE	SHT 39 OF 43	

*** Signal Cross-Reference for the entire design ***

+1_0V_MARVELL 26D2< 27B3>
+1_5V_AGP 12C5< 12D1< 12D4< 15D6< 16C8<
18A2< 18A8< 18C6< 18D5< 19D8< 37C3>
+1_5V_INTREPID_PLL 8D6< 12D4< 12D6< 14D6<> 37D3>
+1_5V_INTREPID_PLL1 14C3< 37D3>
+1_5V_INTREPID_PLL2 14D3< 37D3>
+1_5V_INTREPID_PLL3 14D3< 37D3>
+1_5V_INTREPID_PLL4 14D3< 37D3>
+1_5V_INTREPID_PLL5 12D3< 37D3>
+1_5V_INTREPID_PLL6 12D6< 37D3>
+1_5V_INTREPID_PLL7 8D5< 37D3>
+1_5V_INTREPID_PLL8 14D3< 37C3>
+1_5V_LDO 18A3< 34D8< 37D6>
+1_5V_MAIN 37D6>
+1_5V_MAIN_LX_F 34B8<>
+1_5V_SLEEP 37D6>
+1_5V_SLEEP_VIN 34B6<> 37D6>
+1_8V_MAIN 37D6> 38A2>
+1_8V_MAIN_LX_F 34A4<>
+1_8V_SLEEP 37D6>
+1_95V_FW_DVDD 27C4< 27C7<> 27D5< 37A3>
+1_95V_FW_DVDD_PORT1 27D6< 37A3>
+1_95V_FW_DVDD_RX0 27C5< 37A3>
+1_95V_FW_DVDD_TX0 27C5< 37A3>
+1_95V_FW_PLL400VDD 27D5< 37A3>
+1_95V_FW_PLL500VDD 27D5< 37A3>
+1_95V_FW_PLLVDD 27D5< 27D7<> 37A3>
+2_5V_CG_MAIN 14C5< 37A3>
+2_5V_GPU_FB 18A4< 18A5< 18B4< 18B5< 18C2<
18D2< 18D5< 37C3>
+2_5V_INTREPID 9A8< 10D3< 10D5< 10D7< 10D8< 15D7<
16B8< 37D3>
+2_5V_MAIN 37D6>
+2_5V_MAIN_LX_F 34B2<>
+2_5V_MARVELL 26B8< 26C4<> 37B3>
+2_5V_MARVELL_AVDD 26C4< 37B3>
+2_5V_SLEEP 37D6>
+2_8V_IFP_PLLVDD 37C3>
+3V_CG_PLL_MAIN 14C6< 37A3>
+3V_DAC1VDD 20D4< 37C3>
+3V_DAC2VDD 20D7< 37C3>
+3V_FW 27A3> 27D7<> 28D5< 37B3>
+3V_FW_AVDD 27B4< 37A3>
+3V_FW_AVDD_PORT0 27C6< 37B3>
+3V_FW_AVDD_PORT1 27C6< 37B3>
+3V_FW_AVDD_PORT2 27D6< 37B3>
+3V_FW_ESD 28B3<> 28D2<> 37B3>
+3V_FW_ESD_ILIM 28D4< 37B3>
+3V_FW_LP 27D7<> 37B3>
+3V_GPU 12D1< 14C5< 18A4< 18A8< 18B5<
19A8< 19B2< 19B4< 19C4< 19D2< 20B8<
20C7< 20C8< 20D1< 20D3< 20D3< 20D6<
20D7< 20D7< 37C3>
+3V_GPU_AVDD8 19B4< 37C3>
+3V_GPU_AVDD1 19B2< 37C3>
+3V_GPU_DVO 20B6< 37C3>
+3V_GPU_PLLVDD 20D6< 37C3>
+3V_GPU_PLLVDD8 19A4<
+3V_GPU_SS 20D4< 37C3>
+3V_HALL_EFFECT 22C6<> 37B6> 38C4>
+3V_INTREPID_USB 14C3< 37D3>
+3V_LCD 21B4<> 37B6>
+3V_LCD_SW 21A4< 37B6>
+3V_MAIN 37D6>
+3V_MAIN_LX_F 32D2<>
+3V_NEC_VDD 25D7< 25D7< 37A3>
+3V_PMU 37D6> 38A2>
+3V_PMU_AVCC 29B1< 29B6< 29D5<> 37C6>
+3V_PMU_ESR 31A2< 37C6>
+3V_PMU_RESET 29B7< 33A4<>
+3V_SI_AVCC 20D2< 37B3>
+3V_SI_PLLVCC 20D2< 37B3>
+3V_SI_VCC 20D2< 37B3>
+3V_SLEEP 37D6>
+4_0V_BU 31A3<> 32B5< 37C6>
+4_85V_ESR 31A4< 37C6>
+4_85V_RAW 31A4<> 37C6>
+5V_DDC_SLEEP 21D3<> 21D5<> 37B6> 38A2>
+5V_DDC_SLEEP_UF 21D6< 37B6>
+5V_HD_SLEEP 23D1<> 32A7<> 37C6>
+5V_INV_SW 21B2< 37B6> 38D1>
+5V_INV_UF_SW 21B2< 37B6>
+5V_MAIN 37D6>
+5V_MAIN_LX_F 32D8<>
+5V_SLEEP 37D6>
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+12_8V_INV 21B1< 37B6> 38A2>
+24V_PBUS 37D6> 38B2>
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1_5V_BST 34C5> 37C1>
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BCKFD_PROT_GATE 30D6<>
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CPU_HRESET_L 5B3< 5C2< 7A5< 7A8< 22A2<> 38C8>
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CPU_PLL_FS01 7C4<
CPU_PLL_FS10 7C4<
CPU_PLL_STOP_BASE 7C7<
CPU_PLL_STOP_OC 7C4<> 7C8<> 29B6<>
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CPU_PULLUP 5A3< 5C2<
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CPU_QREQ_L 5B3< 8B6< 8C2< 35D5>
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CPU_VCORE_SEQ_L 33D8<
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CSLOT_ADDR4_SPN 13B7>
CSLOT_ADDR5_SPN 13B7>
CSLOT_ADDR6_SPN 13B7>
CSLOT_ADDR7_SPN 13B7>
CSLOT_ADDR8_SPN 13B7>
CSLOT_ADDR9_SPN 13B7>
CSLOT_CE1_L_SPN 13C7>
CSLOT_CE2_L_SPN 13C7>
CSLOT_IORD_L_SPN 13C7>
CSLOT_IOWAIT_L_PU 13C7<
CSLOT_IOWR_L_SPN 13C7>
CSLOT_OE_L_SPN 13C7>
CSLOT_WE_L_SPN 13C7>
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38C1>
DCDC_EN_L 19C8< 32B6<> 32B6< 34C7<>
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DDR_VREF 11D1< 11D3<> 11D5<> 11D6<> 11D8<>
37D3>
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DVI_DDC_CLK_UF 21C5<> 21D3<> 38C7>
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PMU_PME_L        14B5<> 25B8< 29B2< 29C4<>
PMU_POWERUP_OK   29B4<> 29D2<
PMU_POWER_UP_L   28C7<> 29C6<> 29D7< 32B6<
PMU_REQ_L        1487< 14C2> 29C4<>
PMU_RESET_BUTTON_L  24B2< 29C4<> 29D2<
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PMU_SLEEP_LED    22C4<>
PMU_SLEEP_LED_L  22C2<> 29C4<>
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POWER_UP         28C7<>
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RAM_DATA_A<7>    10B8<> 11D6<>
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RAM_DATA_A<10>   10C7<> 11D8<>
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RAM_DATA_A<55..48>  35B5>
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RAM_DATA_B<63..56>  35A5>
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RAM_DQS_A<2>     10B6<> 11C8<>
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RAM_MUXSEL_L     10A3< 10A5< 10B5<> 10B7<> 35A5>
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RAM_WE_L         9A4< 11B3<> 11B6<> 35A5>
RF_DISABLE_L_SPN  23D6<> 38C1>
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RIGHT_USB_DP     25A3< 31A7<> 36A2> 38D1>
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RJ45_C1_PD       26B2<>
RJ45_C2_PD       26B2<>
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ROM_OE_L         98<  12A5< 23C5<> 38B1>
ROM_ONBOARD_CS_L  98<  23C6<> 38B1>
ROM_RW_L         98<  12A5< 23C6<> 38B1>
ROM_WP_L         98<
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SI_TMDS_DP<1>    20A2> 20B3< 20C1<>
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SLEEP_L_LS5_EN_L  32A5<>
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SND_LIN_SENSE_L  14B5<> 24C7<> 38C6>
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SIZE	DRAWING NUMBER	REV.
D	051-6443	03
SCALE NONE	SHT 41 OF 43	

*** Part Cross-Reference for the entire design ***

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J2	CON_3RTSM_125	24
J3	CON_F14RT_S2MT_SM	23
J4	CON_3RTSM_125	24
J5	CON_12	33
J6	CON_F30RT_S2MT_SM	21
J7	CON_4RT_WRIB	21
J8	CON_F16ST_D_SMA	24
J9	CON_M80ST_D4MT_SM	17
J10	CON_M50SM_5MM	23
J11	CON_F14RT_S2MT_SM	31
J12	CON_F30ST_D_SM	24
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J14	CON_F30RT_T6MT_TH1	21
J15	CON_F5RT_MINIDIN_TH	21
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U3	ADT7460	24
U4	SN74AUC1G08	22
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